4.3V-60V Vin, 5A, High Efficiency Step-down DCDC Converter with Programmable Frequency

FEATURES

- Wide Input Range: 4.3V-60V
- Up to 5A Continuous Output Current
- 0.8V Feedback Reference Voltage
- Integrated 130mΩ High-Side MOSFET
- Ultra Low Quiescent Current: 30uA
- Shutdown Current: 1uA
- Peak current mode control
- Pulse Skipping Mode (PSM) in light load
- 100ns Minimum On-time
- 4ms Internal Soft-start Time
- Frequency Spread Spectrum (FSS) Modulation for EMI Reduction
- Adjustable Frequency and External Clock Synchronization: 100kHz~2.2MHz
- Linear increase in frequency during startup
- Precision Enable Threshold for Programmable Input Voltage Under-Voltage Lock Out Protection (UVLO) Threshold and Hysteresis
- Monotonic Start up with Pre-biased Output
- Hiccup Mode for Over current Protection
- Over-voltage and Over-Temperature Protection
- Available in an ESOP-8 Package

APPLICATIONS

- 12-V, 24-V, 48-V Industry and Telecom Power System
- Industrial Automation and Motor Control
- Vehicle Accessories

DESCRIPTION

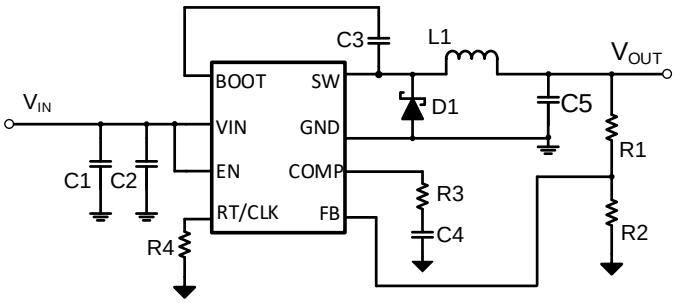
The SCT2650B is 5A buck converter with wide input voltage, ranging from 4.3V to 60V, which integrates an 130mΩ high-side MOSFET. The SCT2650B, adopting the peak current mode control, supports the Pulse Skipping Modulation (PSM) which assists the converter on achieving high efficiency at light load or standby condition.

The switching frequency is programmable from 100kHz to 2.2MHz with two setting modes, resistor setting frequency mode and the clock synchronization mode, to optimizes either the power efficiency or the external components' sizes. The SCT2650B allows power conversion from high input voltage to low output voltage with a minimum 100ns on-time of high-side MOSFET. The SCT2650B is an Electromagnetic Interference (EMI) friendly buck converter with implementing optimized design for EMI reduction. The SCT2650B features Frequency Spread Spectrum FSS with ±6% jittering span and modulation rate 1/512 of switching frequency to reduce the conducted EMI.

The device offers fixed 4ms soft start to prevent inrush current during the startup of output voltage ramping. The SCT2650B supports monotonic start with pre-biased output. The SCT2650B features external loop compensation to provide the flexibility to optimize either loop stability or loop response.

The SCT2650B provides cycle-by-cycle current limit, hiccup mode for over current protection, thermal shutdown protection, output over-voltage protection and input voltage under-voltage protection. The device is available in an 8-pin ESOP-8 package.

TYPICAL APPLICATION



4.3V-60V, Asynchronous Buck Converter

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Release to production.

DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT2650BSTER	Tape & Reel	4000	650B	8	ESOP-8

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN, EN	-0.3	65	V
BOOT	-0.3	71	V
SW	-1	65	V
BOOT-SW	-0.3	6	V
FB, RT/CLK	-0.3	6	V
COMP	-0.3	4	V
Operating junction temperature TJ(2)	-40	150	°C
Storage temperature TSTG	-65	150	°C

PIN CONFIGURATION

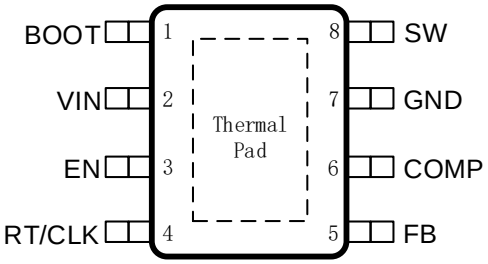


Figure 1. 8-Lead Plastic ESOP

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
BOOT	1	Power supply bias for high-side power MOSFET gate driver. Connect a 0.1uF capacitor from BOOT pin to SW pin. Bootstrap capacitor is charged when SW voltage is low.
VIN	2	Input supply voltage. Connect a local bypass capacitor from VIN pin to GND pin. Path from VIN pin to high frequency bypass capacitor and GND must be as short as possible.
EN	3	Enable pin to the regulator with internal pull-up current source. Pull below 1.05V to disable the converter. Float or connected to VIN through a 100k resistor to enable the converter. The tap of resistor divider from VIN to GND connecting EN pin can adjust the input voltage lockout threshold.
RT/CLK	4	Set the internal oscillator clock frequency or synchronize to an external clock. Connect a resistor from this pin to ground to set switching frequency. An external clock can be input directly to the RT/CLK pin. The internal oscillator synchronizes to the external clock frequency with PLL. If detected clocking edges stops, the operation mode automatically returns to resistor programmed frequency.
FB	5	Inverting input of the trans-conductance error amplifier. The tap of external feedback resistor divider from the output to GND sets the output voltage. The device regulates FB voltage to the internal reference value of 0.8V typical.
COMP	6	Error amplifier output. Connect to frequency loop compensation network.
GND	7	Ground.

SW	8	Regulator switching output. Connect SW to an external power inductor.
Thermal Pad	9	Heat dissipation path of die. Electrically connection to GND pin. Must be connected to ground plane on PCB for proper operation and optimized thermal performance.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted.

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	4.3	60	V
V_{OUT}	Output voltage range	0.8	57	V
T_J	Operating junction temperature	-40	150	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-1	+1	kV
	Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins(2)	-1	+1	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	ESOP-8	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	35.52	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	14.61	
Ψ_{JB}	Junction-to-board characterization parameter(1)	5.65	
$R_{\theta JCtop}$	Junction to case thermal resistance(1)	67.26	
$R_{\theta JB}$	Junction-to-board thermal resistance(1)	15.07	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2650B is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT2650B. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.
(2) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN}=24V, T_J=-40°C~125°C, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Operating input voltage		4.3		60	V
V_{IN_UVLO}	Input UVLO Threshold Hysteresis	V_{IN} rising		4 200	4.25	V mV
I_{SHDN}	Shutdown current from VIN pin	EN=0, no load		1	5	μA
I_Q	Quiescent current from VIN pin	EN floating, no load, non-switching, BOOT-SW=5V		30		μA
Power MOSFETs						
R_{DSON_H}	High-side MOSFET on-resistance	V_{BOOT}-V_{SW}=5V		130		mΩ
Reference and Control Loop						
V_{REF}	Reference voltage of FB	Tj=25°C	0.792	0.8	0.808	V
		Tj=-40°C ~125°C	0.788		0.812	V
G_{EA}	Error amplifier trans-conductance	-2μA<I_{COMP}<2μA, V_{COMP}=1V		200		μS
I_{COMP_SRC}	EA maximum source current	V_{FB}=V_{REF}-100mV, V_{COMP}=1V		30		μA
I_{COMP_SNK}	EA maximum sink current	V_{FB}=V_{REF}+100mV, V_{COMP}=1V		30		μA
V_{COMP_H}	COMP high clamp			2.4		V
V_{COMP_L}	COMP low clamp			0.4		V
Current Limit and Over Current Protection						
I_{LIM_HS}	High-side power MOSFET peak current limit threshold	Tj=25°C	7.45	7.8	8.15	A
		Tj=-40°C ~125°C	7.07		8.47	A
T_{HIC_W}	Over current protection hiccup wait time			512		cycles
T_{HIC_R}	Over current protection hiccup restart time			8192		cycles
Enable and Soft Startup						
V_{EN_H}	Enable high threshold		1.1	1.2	1.3	V
V_{EN_L}	Enable low threshold		0.9	1.05	1.2	V
I_{EN_L}	Enable pin pull-up current	EN=1V		1		μA
I_{EN_H}	Enable pin pull-up current	EN=1.5V		4		uA
T_{SS}	Soft start time			4		ms
Switching Frequency and External Clock Synchronization						
F_{RANGE_RT}	Frequency range using RT mode		100		2200	kHz
F_{SW}	Switching frequency	R_{RT}=200 kΩ(1%), Tj=25°C	470	500	530	kHz
		R_{RT}=200 kΩ(1%), Tj=-40°C ~125°C	435		565	
t_{ON_MIN}	Minimum on-time	V_{IN}=24V		100		ns
Protection						
V_{OVP}	Feedback overvoltage with respect to reference voltage	V_{FB}/V_{REF} rising V_{FB}/V_{REF} falling		110 105		% %
V_{BOOTUV}	BOOT-SW UVLO threshold	BOOT-SW falling Hysteresis		2.5 300		V mV

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
T_{SD}	Thermal shutdown threshold *	T_J rising		175		°C
		Hysteresis		15		°C

*Derived from bench characterization

TYPICAL CHARACTERISTICS

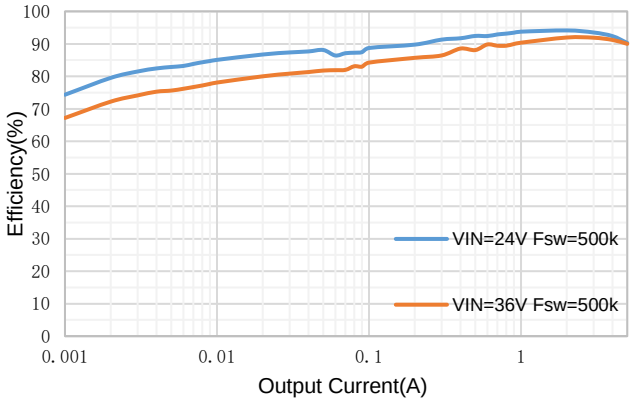


Figure 2. Efficiency vs Load Current, Vout=12V

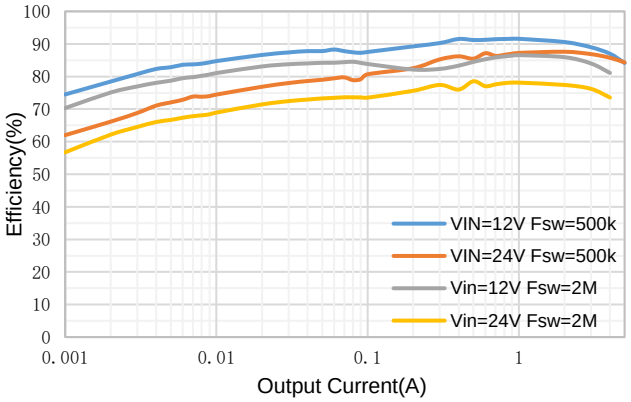


Figure 3. Efficiency vs Load Current, Vout=5V

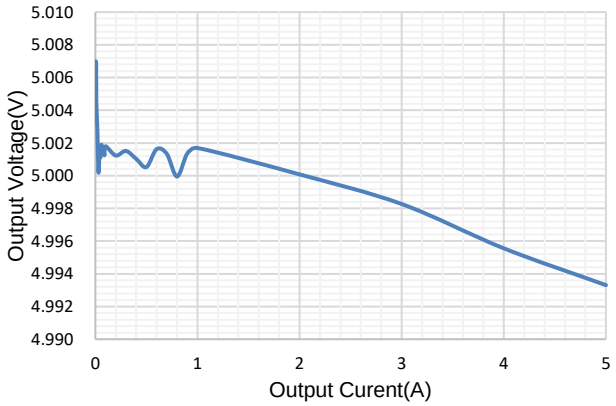


Figure 4. Load Regulation, Vin=24V, Vout=5V, Fsw=500k

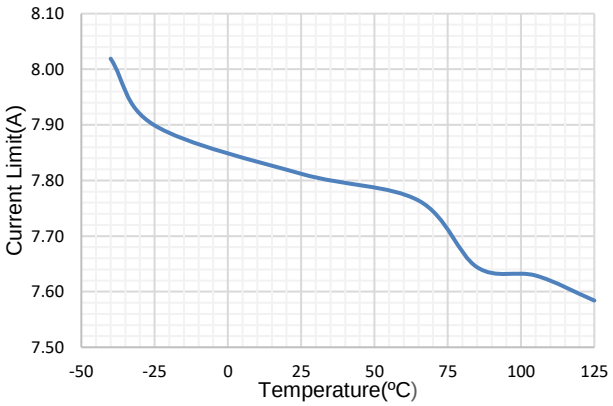


Figure 5. Current Limit VS Temperature

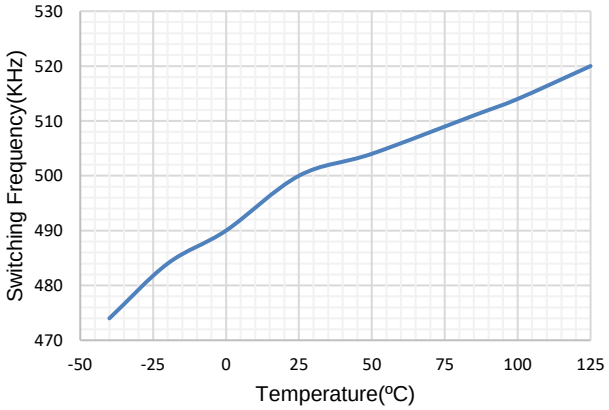


Figure 6. Switching Frequency VS Temperature

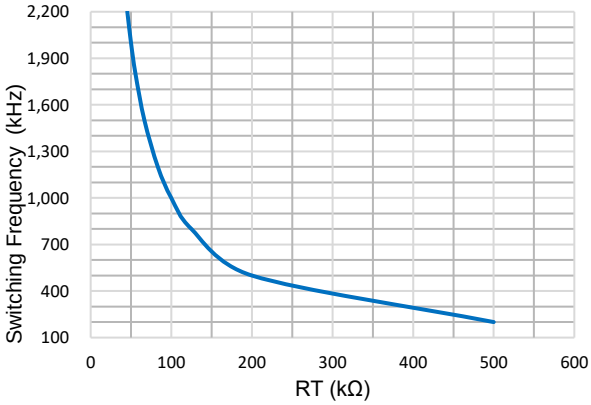


Figure 7. Switching Frequency vs RT Resistor

FUNCTIONAL BLOCK DIAGRA

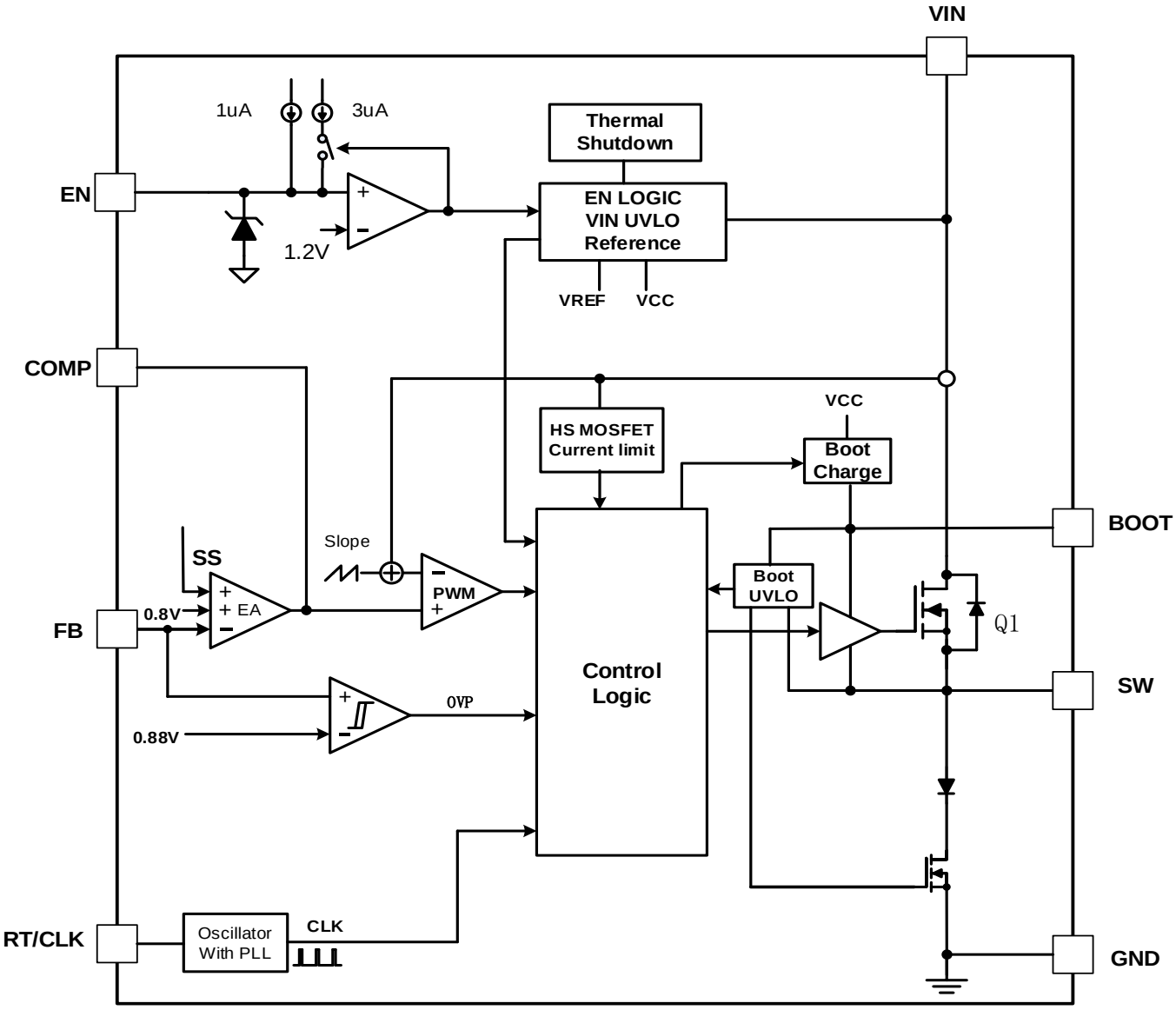


Figure 8. Functional Block Diagram

OPERATION

Overview

The SCT2650B is a 4.3V-60V input, 5A output, buck converter with integrated 130mΩ Rdson high-side power MOSFET. It implements constant frequency peak current mode control to regulate output voltage, providing excellent line and load transient response and simplifying the external loop compensation design.

The switching frequency is programmable from 100kHz to 2.2MHz with two setting modes, resistor setting frequency mode and the clock synchronization mode, to optimizes either the power efficiency or the external components' sizes. The SCT2650B features an internal 4ms soft-start time to avoid large inrush current and output voltage overshoot during startup. The device also supports monolithic startup with pre-biased output condition. The seamless mode-transition between PWM mode and PSM mode operations ensure high efficiency over wide load current range. The quiescent current is typically 30uA under no load or sleep mode condition to achieve high efficiency at light load. The SCT2650B will experience a linear increase in frequency during startup.

The SCT2650B has a default input start-up voltage of 4V with 200mV hysteresis. The EN pin is a high-voltage pin with a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher UVLO system requirements. Floating EN pin enables the device with the internal pull-up current to the pin. Connecting EN pin to VIN directly starts up the device automatically.

The SCT2650B implements the Frequency Spread Spectrum FSS modulation spreading of ±6% centered selected switching frequency. FSS improves EMI performance by not allowing emitted energy to stay in any one receiver band for a significant length of time.

The SCT2650B full protection features include the input under-voltage lockout, the output over-voltage protection, over current protection with cycle-by-cycle current limiting and hiccup mode, output hard short protection and thermal shutdown protection.

Peak Current Mode Control

The SCT2650B employs fixed frequency peak current mode control. An internal clock initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly. When the current through high-side MOSFET reaches the threshold level set by the COMP voltage of the internal error amplifier, the integrated high-side MOSFET is turned off.

The error amplifier serves the COMP node by comparing the voltage of the FB pin with an internal 0.8V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage to the reference. The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

The SCT2650B operates in Pulse Skipping Mode (PSM) with light load current to improve efficiency. When the load current decreases, an increment in the feedback voltage leads COMP voltage drop. When COMP falls to a low clamp threshold (400mV typically), device enters PSM. The output voltage decays due to output capacitor discharging during skipping period. Once FB voltage drops lower than the reference voltage, and the COMP voltage rises above low clamp threshold. Then high-side power MOSFET turns on in next clock pulse. After several switching cycles with typical 600mA peak inductor current, COMP voltage drops and is clamped again and pulse skipping mode repeats if the output continues light loaded.

This control scheme helps achieving higher efficiency by skipping cycles to reduce switching power loss and gate drive charging loss. The controller consumption quiescent current is 30uA during skipping period with no switching to improve efficiency further.

Enable and Under Voltage Lockout Threshold

The SCT2650B is enabled when the VIN pin voltage rises above 4V and the EN pin voltage exceeds the enable threshold of 1.2V. The device is disabled when the VIN pin voltage falls below 3.8V or when the EN pin voltage is below 1.05V. An internal 1uA pull up current source to EN pin allows the device enable when EN pin floats.

EN pin is a high voltage pin that can be connected to VIN directly to start up the device.

For a higher system UVLO threshold, connect an external resistor divider (R1 and R2) shown in Figure 9 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

$$R1 = \frac{V_{rise} * 0.875 - V_{fall}}{3.125uA} \quad (1)$$

$$R2 = \frac{R_1 * 1.05}{V_{fall} - 1.05 + R_1 * 4uA} \quad (2)$$

where

- V_{rise} is rising threshold of Vin UVLO
- V_{fall} is falling threshold of Vin UVLO

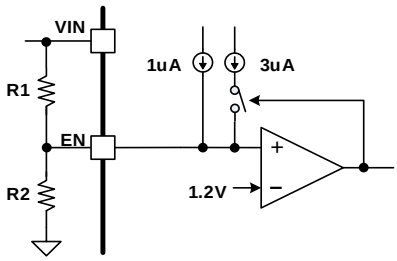


Figure 9. System UVLO by enable divide

Output Voltage

The SCT2650B regulates the internal reference voltage at 0.8V over the operating temperature and voltage range. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

$$R_{FB\_TOP} = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_{FB\_BOT} \quad (3)$$

where

- R_{FB_TOP} is the resistor connecting the output to the FB pin.
- R_{FB_BOT} is the resistor connecting the FB pin to the ground.

Internal Soft-Start

The SCT2650B integrates an internal soft-start circuit that ramps the reference voltage from zero volts to 0.8V reference voltage in 4ms. If the EN pin is pulled below 1.05V, switching stops and the internal soft-start resets. The soft-start also resets during shutdown due to thermal overloading.

Switching Frequency and Clock Synchronization

The switching frequency of the SCT2650B is set by placing a resistor between RT/CLK pin and the ground or synchronizing to an external clock.

In resistor setting frequency mode, a resistor placed between RT/CLK pin to the ground sets the switching frequency over a wide range from 100KHz to 2.2MHz. The RT/CLK pin voltage is typical 0.5V. RT/CLK pin is not allowed to be left floating or shorted to the ground. Use Equation 4 or the plot in Figure 10. to determine the resistance for a switching frequency needed.

$$RT(K\Omega) = \frac{100000}{fsw(KHz)} \quad (4)$$

where, fsw is switching clock frequency

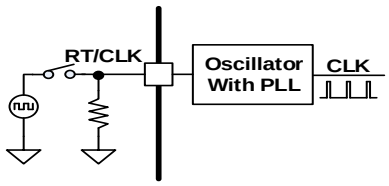


Figure 10. Setting Frequency and Clock Synchronization

In clock synchronization mode, the switching frequency synchronizes to an external clock applied to RT/CLK pin. The synchronization frequency range is from 100KHz to 2.2MHz and the rising edge of the SW synchronizes to the

falling edge of the external clock at RT/CLK pin with typical 66ns time delay. A square wave clock signal to RT/CLK pin must have high level no lower than 3.5V, low level no higher than 0.4V, and pulse width larger than 80ns.

In applications where both resistor setting frequency mode and clock synchronization mode are needed, the device can be configured as shown in Figure 10. Before an external clock is present, the device works in resistor setting frequency mode. When an external clock presents, the device automatically transitions from resistor setting mode to external clock synchronization mode. An internal phase locked loop PLL locks internal clock frequency onto the external clock within typical 85us. The converter transitions from the clock synchronization mode to the resistor setting frequency mode when the external clock disappears.

Frequency Spread Spectrum

To reduce EMI, the SCT2650B implements Frequency Spread Spectrum (FSS). The FSS circuitry shifts the switching frequency of the regulator periodically within a certain frequency range around the adjusted switching frequency. The jittering span is ±6% of the switching frequency with 1/512 swing frequency.

Linear Frequency Reduction

In order to optimize the performance of the output voltage during startup and optimize the inductance current ripple, the SCT2650B adopts a linear frequency reduction function design during startup power-up. During the process of increasing the FB pin voltage from 0V to 0.8V during startup, the frequency of SCT2650B will linearly increase to the set frequency in a certain proportion.

Bootstrap Voltage Regulator and Low Drop-out Operation

An external bootstrap capacitor between BOOT pin and SW pin powers the floating gate driver to high-side power MOSFET. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and the external low-side diode conducts. The recommended value of the BOOT capacitor is 0.1 μF.

The UVLO of high-side MOSFET gate driver has rising threshold of 2.5V and hysteresis of 300mV. When the device operates with high duty cycle or extremely light load, bootstrap capacitor may be not recharged in considerable long time. The voltage at bootstrap capacitor is insufficient to drive high-side MOSFET fully on. When the voltage across bootstrap capacitor drops below 2.2V, BOOT UVLO occurs. The converter forces turning on an integrated low-side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee the converter's operation over a wide duty range.

During the condition of ultra-low voltage difference from the input to the output, SCT2650B operates in Low Drop-Out LDO mode. High-side MOSFET remains turning on as long as the BOOT pin to SW pin voltage is higher than BOOT UVLO threshold 2.5V, during which the switching frequency decreases and the duty cycle increases. To avoid audio interference and maintain the voltage of the bootstrap capacitor, the switching frequency will not be lower than 75kHz. The high side MOSFET only turns off for 200ns in each switching cycle to minimize output voltage ripple while charging the bootstrap capacitor. The effective duty cycle of the converter during LDO operation can approach 100%.

During slowing power up and power down application, the output voltage can closely track the input voltage ramping down thanks to LDO operation mode. As the input voltage is reduced to near the output voltage, i.e., during slowing power-up and power-down application, the off-time of the high side MOSFET starts to approach the minimum value. Without LDO operation mode, beyond this point the switching may become erratic and/or the output voltage will fall out of regulation. To avoid this problem, the SCT2650B LDO mode automatically reduces the switching frequency to increase the effective duty cycle and maintain regulation.

Over Current Limit and Hiccup Mode

The SCT2650B implements over current protection with fold back current limit. The SCT2650B cycle-by-cycle limits high-side MOSFET peak current to avoid inductor current running away during unexpected overload or output hard short condition.

When overload or hard short happens, the converter cannot provide output current to satisfy loading requirement. The inductor current is clamped at over current limitation. Thus, the output voltage drops below regulated voltage

with FB voltage less than internal reference voltage continuously. The COMP pin voltage ramps up to high clamp voltage 2.4V typical. When FB voltage is below 40% of V_{REF} for 512 cycles, the converter stops switching. After remaining OFF for 8192 cycles, the device restarts from soft starting phase. If overload or hard short condition still exists during soft-start and make FB voltage is below 40% of V_{REF} for 512 cycles, the device enters turning-off mode again. When overload or hard short condition is removed, the device automatically recovers to enters normal regulating operation.

The hiccup protection mode above makes the average short circuit current to alleviate thermal issues and protect the regulator.

The SCT2650B implements frequency foldback to protect the converter in unexpected overload or output hard short condition at higher switching frequencies and input voltages. The oscillator frequency is divided by 1, 2, 4, and 8 as the FB pin voltage falls from 0.8 V to 0 V. The SCT2650B uses a digital frequency foldback to enable synchronization to an external clock during normal start-up and fault conditions. During short-circuit events, the inductor current can exceed the peak current limit because of the high input voltage and the minimum on-time. When the output voltage is forced low by the shorted load, the inductor current decreases slowly during the switch off-time. The frequency foldback effectively increases the off time by increasing the period of the switching cycle providing more time for the inductor current to ramp down.

With a maximum frequency foldback ratio of 8, there is a maximum frequency at which the inductor current can be controlled by frequency foldback protection. Equation 5 calculates the maximum switching frequency at which the inductor current remains under control when V_{OUT} is forced to V_{OUT_SHORT}. The selected operating frequency must not exceed the calculated value.

$$f_{sw(\max skip)} = \frac{f_{DIV}}{t_{min\_ON}} \times \left(\frac{I_{LIMIT} \times R_{DC} + V_{OUT\_SHORT} + V_d}{V_{IN\_MAX} - I_{LIMIT} \times R_{DS(on)} + V_d}\right) \quad (5)$$

where

I_{LIMIT}: Limited average current

R_{DC}: Inductor DC resistance

V_{IN_MAX}: Maximum input voltage

V_{OUT_SHORT}: Output voltage during short

V_d: Diode voltage drop

$R_{DS(on)}$: Integrated high side FET on resistance

T_{min_ON}: Controllable minimum on time

f_{DIV}: Frequency divide equals (1,2,4 or 8)

Over voltage Protection

The SCT2650B implements the Over-voltage Protection OVP circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. The overvoltage comparator in OVP circuit compares the FB pin voltage to the internal reference voltage. When FB pin voltage exceeds 110% of internal 0.8V reference voltage, the high-side MOSFET turns off to avoid output voltage continue to increase. When the FB pin voltage falls below 105% of the 0.8V reference voltage, the high-side MOSFET can turn on again.

Thermal Shutdown

The SCT2650B protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 175°C, the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 160°C, the device restarts with internal soft start phase.

APPLICATION INFORMATION

Typical Application

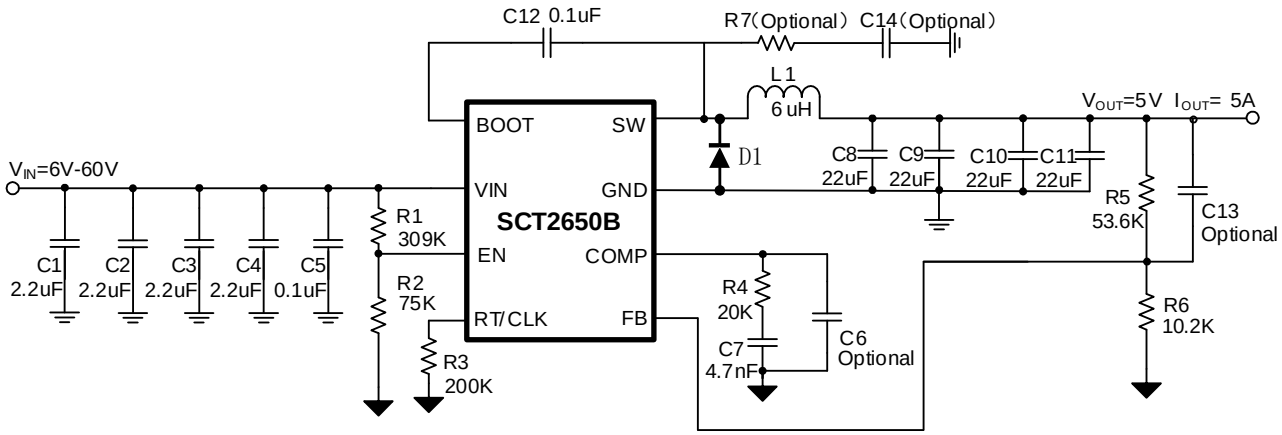


Figure 11. SCT2650B Design Example, 5V Output with Programmable UVLO

Design Parameters

Design Parameters	Example Value
Input Voltage	24V Normal, 6V to 60V
Output Voltage	5V
Maximum Output Current	5A
Switching Frequency	500 KHz
Output voltage ripple (peak to peak)	10.4mV
Transient Response 1.25A to 3.75A load step	ΔVout = 420mV
Start Input Voltage (rising VIN)	5.8V
Stop Input Voltage (falling VIN)	4.1V

Output Voltage

The output voltage is set by an external resistor divider R5 and R6 in typical application schematic. Recommended R6 resistance is 10.2KΩ. Use Equation 6 to calculate R5.

$$R_5 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_6 \quad (6)$$

where:

- V_{REF} is the feedback reference voltage, typical 0.8V.

Table 1. R_5, R_6Value for Common Output Voltage (Room Temperature)

V_{OUT}	R_5	R_6
3.3 V	31.6 KΩ	10.2 KΩ
5 V	53.6 KΩ	10.2 KΩ
12 V	143 KΩ	10.2 KΩ
24 V	294 KΩ	10.2 KΩ

Switching Frequency

Higher switching frequencies support smaller profiles of output inductors and output capacitors, resulting in lower voltage and current ripples. However, the higher switching frequency causes extra switching loss, which downgrades converter's overall power efficiency and thermal performance. The 100ns minimum on-time limitation also restricts the selection of higher switching frequency. In this design, a moderate switching frequency of 500 kHz is selected to achieve both small solution size and high efficiency operation.

The resistor connected from RT/CLK to GND sets switching frequency of the converter. The resistor value required for a desired frequency can be calculated using Equation 7 or determined from table 2.

$$R_3(\mathrm{K\Omega}) = \frac{100000}{\text{fsw (KHz)}} \quad (7)$$

where:

- f_{SW} is the desired switching frequency.

Table 2. R_{FSW} Value for Common Switching Frequencies (Room Temperature)

Fsw	R_3 (R_{FSW})
200 KHz	500 KΩ
500 KHz	200 KΩ
800 KHz	125 KΩ
1200 KHz	83 KΩ
2000 KHz	49.9 KΩ
2200 KHz	45.3 KΩ

Under Voltage Lock-Out

An external voltage divider network of R_1 from the input to EN pin and R_2 from EN pin to the ground can set the input voltage's Under Voltage Lock-Out (UVLO) threshold. The UVLO has two thresholds, one for power up when the input voltage is rising and the other for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 5.8V (start or enable). After the regulator starts switching, it should continue to do so until the input voltage falls below 4.1V (stop or disable). Use Equation 8 and Equation 9 to calculate the values 309 kΩ and 75 kΩ of R_1 and R_2 resistors.

$$R1 = \frac{V_{rise} * 0.875 - V_{fall}}{3.125uA} \quad (8)$$

$$R2 = \frac{R_1 * 1.05}{V_{fall} - 1.05 + R_1 * 4uA} \quad (9)$$

Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance (DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 20%~40% of the maximum output current.

The peak-to-peak ripple current in the inductor I_{LPP} can be calculated as in Equation 10.

$$I_{LPP} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{V_{IN} * L * f_{SW}} \quad (10)$$

Where:

- I_{LPP} is the inductor peak-to-peak current.
- L is the inductance of inductor.
- f_{SW} is the switching frequency.
- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 11 to calculate the inductance value.

$$L_{MIN} = \frac{V_{OUT}}{f_{SW} * LIR * I_{OUT(max)}} * (1 - \frac{V_{OUT}}{V_{IN(max)}}) \quad (11)$$

Where:

- L_{MIN} is the minimum inductance required.
- f_{sw} is the switching frequency.
- V_{OUT} is the output voltage.
- $V_{IN(max)}$ is the maximum input voltage.
- $I_{OUT(max)}$ is the maximum DC load current.
- LIR is coefficient of I_{LPP} to I_{OUT}.

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in Equation 12 and Equation 13.

$$I_{LPEAK} = I_{OUT} + \frac{I_{LPP}}{2} \quad (12)$$

$$I_{LRMS} = \sqrt{(I_{OUT})^2 + \frac{1}{12} * (I_{LPP})^2} \quad (13)$$

Where:

- I_{LPEAK} is the inductor peak current.
- I_{OUT} is the DC load current.
- I_{LPP} is the inductor peak-to-peak current.
- I_{LRMS} is the inductor RMS current.

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 7.8A. The most conservative approach is to choose an inductor with a saturation current rating greater than 7.8A. Because of the maximum I_{LPEAK} limited by device, the maximum output current that the SCT2650B can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also

affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a lower maximum output current.

Diode Selection

The SCT2650B requires an external catch diode between the SW pin and GND. The selected diode must have a reverse voltage rating equal to or greater than VIN (max). The peak current rating of the diode must be greater than the maximum inductor current. Schottky diodes are typically a good choice for the catch diode due to their low forward voltage. The lower the forward voltage of the diode, the higher the efficiency of the regulator.

Typically, diodes with higher voltage and current ratings have higher forward voltages. A diode with a minimum of 60-V reverse voltage is preferred to allow input voltage transients up to the rated voltage of the SCT2650B.

For the example design, the PDS760-13 Schottky diode is selected for its lower forward voltage and good thermal characteristics compared to smaller devices. The typical forward voltage of the PDS760-13 is 0.48 volts at 5A.

The diode must also be selected with an appropriate power rating. The diode conducts the output current during the off time of the internal power switch. The off time of the internal switch is a function of the maximum input voltage, the output voltage, and the switching frequency. The output current during the off time is multiplied by the forward voltage of the diode to calculate the instantaneous conduction losses of the diode. At higher switching frequencies, the ac losses of the diode need to be considered. The ac losses of the diode are due to the charging and discharging of the junction capacitance and reverse recovery charge. Equation 14 is used to calculate the total power dissipation, including conduction losses and ac losses of the diode.

The PDS760-13 diode has a junction capacitance of 400 pF. Using Equation 14, the total loss in the diode at the maximum input voltage is 1.9W.

If the power supply spends a significant amount of time at light load currents or in sleep mode, consider using a diode which has a low leakage current and slightly higher forward voltage drop.

$$P_D = \frac{(V_{IN\_MAX} - V_{OUT}) \times I_{OUT} \times V_d}{V_{IN\_MAX}} + \frac{C_j \times f_{SW} \times (V_{IN} + V_d)^2}{2} \quad (14)$$

Input Capacitor Selection

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g., 0.1uF) with small package size (0603) to filter high frequency switching noise. Place the small size capacitor as close to VIN and GND pins as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input capacitor can be calculated using Equation 15.

$$\mathrm{I_{CINRMS}} = \mathrm{I_{OUT}} * \sqrt{\frac{\mathrm{V_{OUT}}}{\mathrm{V_{IN}}} * (1 - \frac{\mathrm{V_{OUT}}}{\mathrm{V_{IN}}})} \quad (15)$$

The worst case condition occurs at V_{IN}=2*V_{OUT}, where:

$$\mathrm{I_{CINRMS}} = 0.5 * \mathrm{I_{OUT}} \quad (16)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increasing.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 17 and the maximum input voltage ripple occurs at 50% duty cycle.

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} * C_{IN}} * \frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}}) \quad (17)$$

For this example, four 2.2μF, X7R ceramic capacitors rated for 100 V in parallel are used. And a 0.1 μF for high-frequency filtering capacitor is placed as close as possible to the device pins.

Bootstrap Capacitor Selection

A 0.1μF ceramic capacitor must be connected between BOOT pin and SW pin for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 18 desired.

$$\Delta V_{OUT} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{8 * {f_{SW}}^2 * L * C_{OUT} * V_{IN}} \quad (18)$$

Where:

- $\Delta V_{OUT}$is the output voltage ripple.
- f_{SW} is the switching frequency.
- L is the inductance of inductor.
- C_{OUT} is the output capacitance.
- V_{OUT} is the output voltage.
- $V_{IN}$is the input voltage.

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, four 22μF ceramic output capacitors work for most applications.

Compensation Components

The SCT2650B employs peak current mode control for easy compensation and fast transient response. An external network comprising resister R4, ceramic capacitors C7 and optional C6 connected to the COMP pin is used for the loop compensation. The Equation 19 shows the close-loop small signal transfer function.

$$H(S) = \left[A_{EA} * \frac{1 + \frac{S}{2\pi * f_{Z1}}}{\left(1 + \frac{S}{2\pi * f_{P1}}\right) * \left(1 + \frac{S}{2\pi * f_{P3}}\right)}\right] * \left[G_{ISNS} * \frac{V_{OUT}}{I_{OUT}} * \frac{1 + \frac{S}{2\pi * f_{Z2}}}{1 + \frac{S}{2\pi * f_{P2}}}\right] * \frac{V_{FB}}{V_{OUT}} \quad (19)$$

Where:

- A_{EA} is error amplifier voltage gain.
- G_{ISNS} is COMP to SW current trans-conductance, 22A/V typically.

The DC voltage gain of the loop is given by Equation 20.

$$A_{VDC} = A_{EA} * G_{ISNS} * \frac{V_{FB}}{I_{OUT}} \quad (20)$$

The system has two noteworthy poles: one is due to the compensation capacitor C7 and the error amplifier output resistor. The other is caused by the output capacitor and the load resistor. These poles as located at:

$$f_{P1} = \frac{1}{2\pi * R_{OEA} * C_7} = \frac{G_{EA}}{2\pi * A_{EA} * C_7} \quad (21)$$

$$f_{P2} = \frac{1}{2\pi * R_{LOAD} * C_{OUT}} = \frac{I_{OUT}}{2\pi * V_{OUT} * C_{OUT}} \quad (22)$$

Where:

- R_{OEA} is error amplifier output resistor.
- G_{EA} is Error amplifier trans-conductance, 200uS typically.
- R_{LOAD} is equivalent load resistor.

The system has one zero of importance from R4 and C7. fz1 is used to counteract the fp2, and fz1 located at:

$$f_{Z1} = \frac{1}{2\pi * C_7 * R_4} \quad (23)$$

The system may have another important zero if the output capacitor has a large capacitance or a high ESR value. The zero, due to the ESR and the capacitance of the output capacitor is calculated by Equation 24.

$$f_{Z2} = \frac{1}{2\pi * C_{OUT} * ESR} \quad (24)$$

In this case, a third pole set by the optional compensation capacitor C6 and the compensation resistor R4 is used to compensates the effect of the ESR zero. This pole is calculated by Equation 25.

$$f_{P3} = \frac{1}{2\pi * C_6 * R_4} \quad (25)$$

The crossover frequency of converter is shown in Equation 26.

$$f_C = \frac{V_{FB}}{V_{OUT}} * \frac{G_{EA} * G_{ISNS} * R_4}{2\pi * C_{OUT}} \quad (26)$$

The system crossover frequency, where the feedback loop has unity gain, is important. A lower crossover frequency results in slower line and load transient response. A higher crossover frequency could cause the system unstable. A recommended rule of thumb is to set the crossover frequency to be approximately 1/10 of switching frequency.

The following steps can be followed to calculate the external compensation components. Calculate the compensation resistor R4 with Equation 27 once crossover frequency is selected.

$$R_4 = \frac{V_{OUT}}{V_{FB}} * \frac{2\pi * C_{OUT} * f_C}{G_{EA} * G_{ISNS}} \quad (27)$$

Then calculate C7 by placing a compensation zero at or before the output stage pole.

$$C_7 = \frac{R_{LOAD} * C_{OUT}}{R4} \quad (28)$$

Determine if the optional compensation capacitor C6 is required. Generally, it is required if the ESR zero f_{Z2} is located less than half of the switching frequency. Then fp3 can be used to cancel fz2. C6 can be calculated with Equation 29.

$$C_6 = \frac{C_{OUT} \times ESR}{R_4} \quad (29)$$

Table 3 lists typical values of compensation components for some standard output voltages with various output ceramic capacitors and inductors. The values of the compensation components have been optimized for fast transient responses and good stability. For the conditions do not list in Table 3, customers can use Equation 27-Equation 29 to optimize the compensation components.

Table 3: Compensation Values for Typical Output Voltage/Capacitor Combinations

Vout	Fsw	R3	L1	COUT	R4	C7	C6
5V	500K	200KΩ	6uH	4*47uF	20K	4.7nF	optional
5V	2M	50KΩ	1.5uH	4*47uF	20K	4.7nF	optional
12V	500K	200KΩ	10uH	4*47uF	33.2K	3.3nF	optional
12V	2M	50KΩ	3.3uH	4*47uF	33.2K	3.3nF	optional
24V	500K	200KΩ	15uH	4*47uF	45.3k	2.2nF	220pF
24V	2M	50KΩ	4.7uH	4*47uF	45.3k	2.2nF	220pF

Inverting Power application

The SCT2650B can be used to convert a positive input voltage to a negative output voltage. Typical applications are amplifiers requiring a negative power supply.

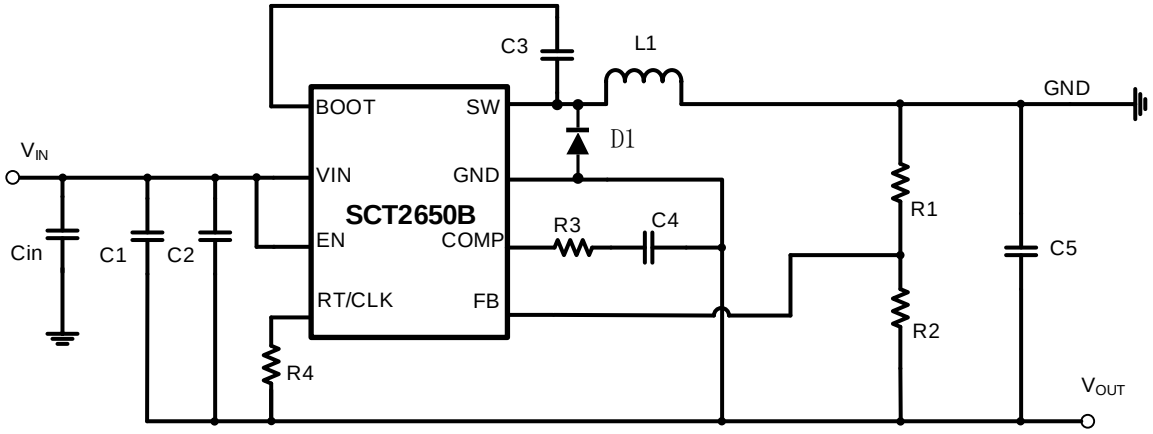


Figure 12. SCT2650B Inverting Power Supply

Application Waveforms

V_{IN}=24V, V_{OUT}=5V, F_{SW}=500k, unless otherwise noted

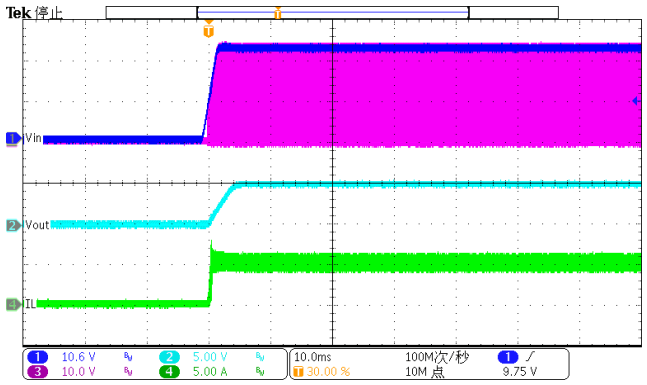


Figure 13. Power up (I_{LOAD}=5A)

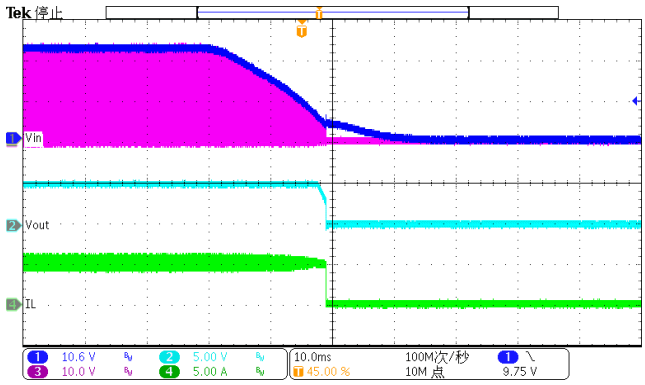


Figure 14. Power down (I_{LOAD}=5A)

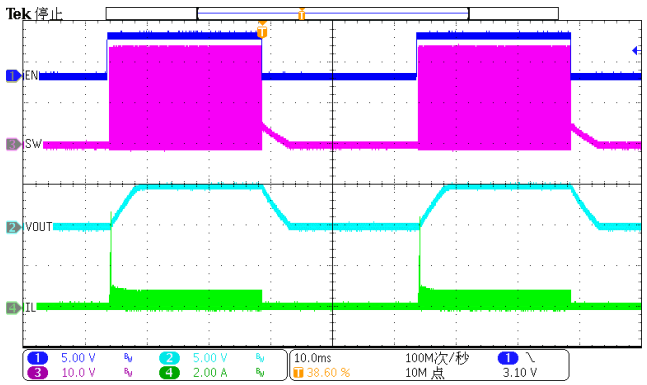


Figure 15. EN toggle (I_{LOAD}=0.1A)

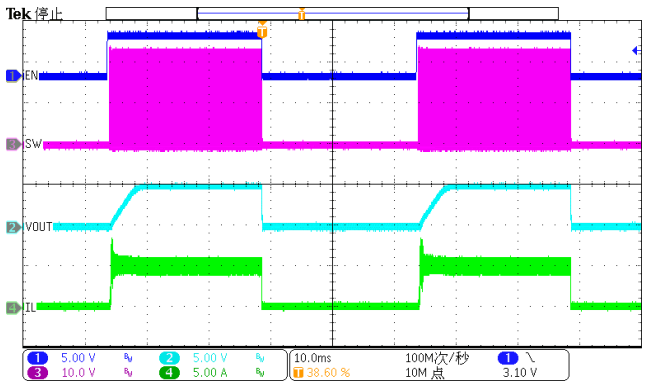


Figure 16. EN toggle (I_{LOAD}=5A)

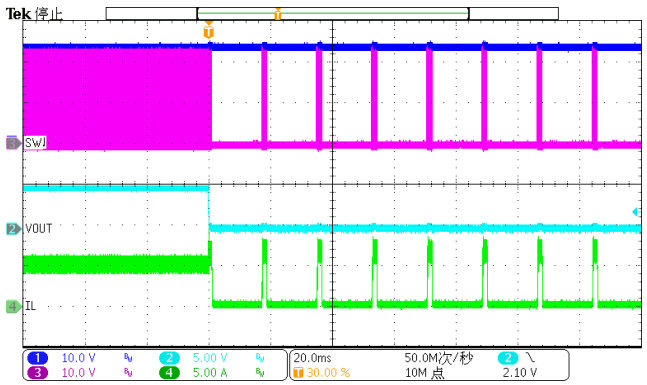


Figure 17. Over Current Protection (5A to hard short)

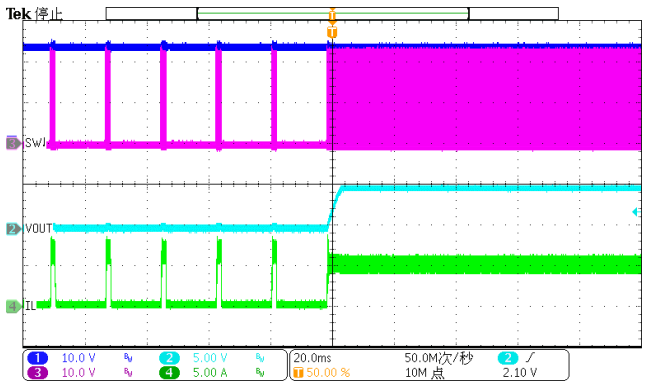


Figure 18. Over Current Release (hard short to 5A)

Application Waveforms

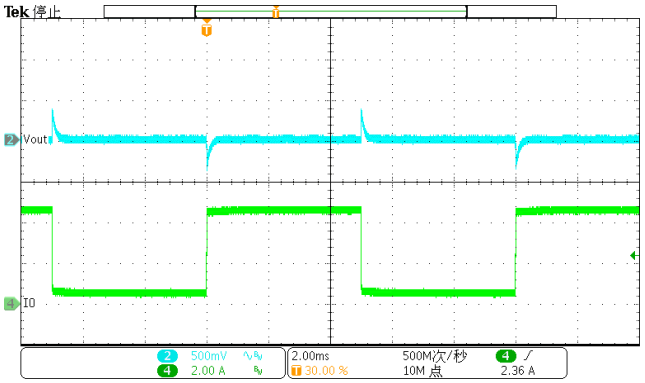


Figure 19. Load Transient (0.5A-4.5A, 1.6A/us)

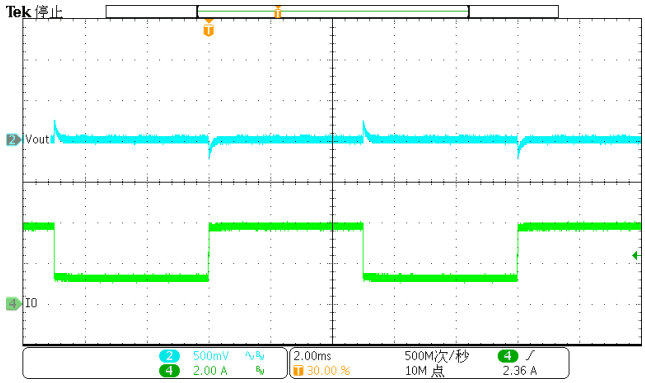


Figure 20. Load Transient (1.25A-3.75A, 1.6A/us)

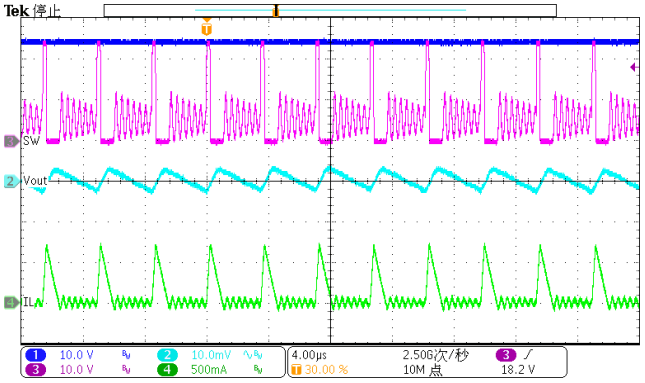


Figure 21. Output Ripple (I_{LOAD}=100mA)

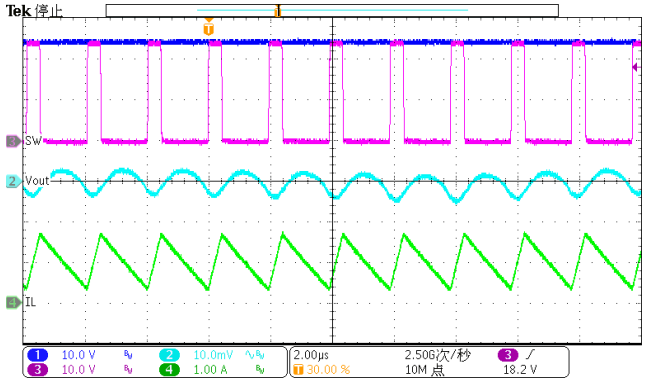


Figure 22. Output Ripple (I_{LOAD}=1A)

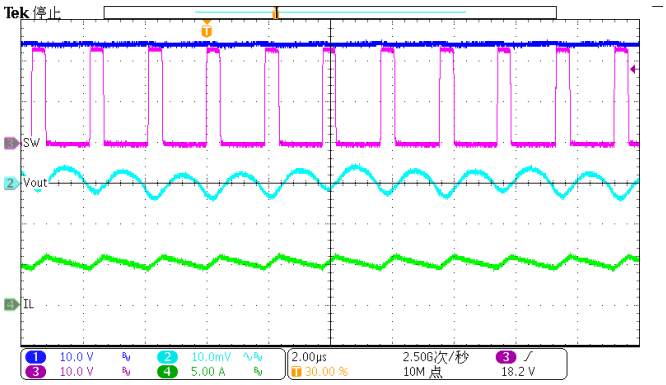


Figure 23. Output Ripple (I_{LOAD}=5A)

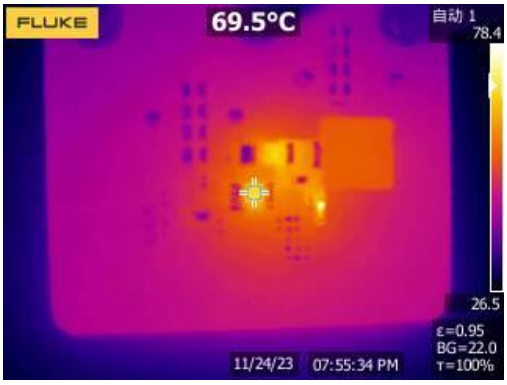


Figure 24. Thermal, 24V_{IN}, 5V_{OUT}, 3.5A

Layout Guideline

Proper PCB layout is a critical for SCT2650B's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing overheat area.
2. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
3. Freewheeling diode should be place as close to SW pin and the ground as possible to reduce parasitic effect.
4. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.
5. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground planes using multiple vias directly under the IC. The center thermal pad should always be soldered to the board for mechanical strength and reliability, using multiple thermal vias underneath the thermal pad. Improper soldering thermal pad to ground plate on PCB will cause SW higher ringing and overshoot besides downgrading thermal performance. it is recommended 10mil diameter drill holes of thermal vias, but a smaller via offers less risk of solder volume loss. On applications where solder volume loss thru the vias is of concern, plugging or tenting can be used to achieve a repeatable process.
6. Output inductor and freewheeling diode should be placed close to the SW pin. The switching area of the PCB conductor minimized to prevent excessive capacitive coupling.
7. The RT/CLK terminal is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace.
8. UVLO adjust and RT resistors, loop compensation and feedback components should connect to small signal ground which must return to the GND pin without any interleaving with power ground.
9. Route BOOT capacitor trace on the other layer than top layer to provide wide path for topside ground.
10. For achieving better thermal performance, a four-layer layout is strongly recommended.

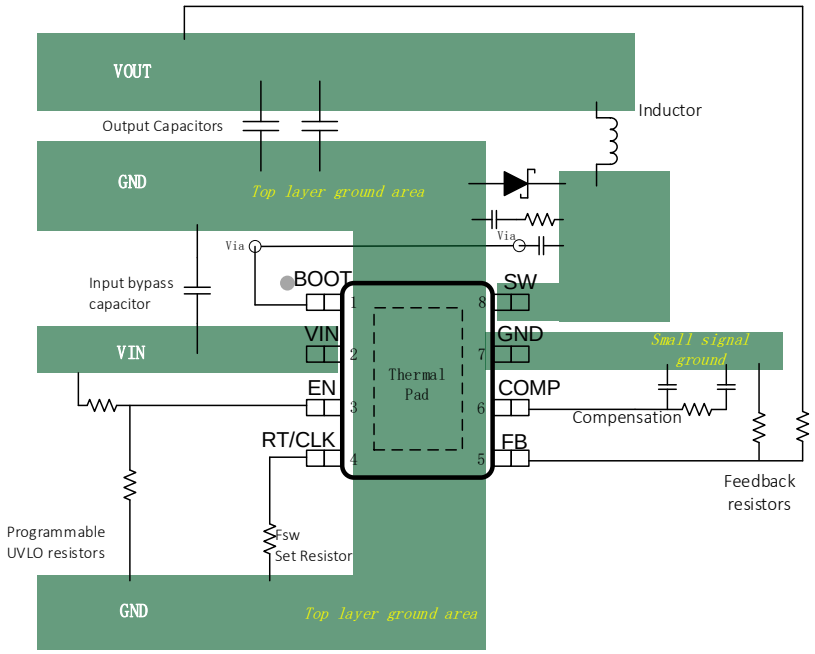
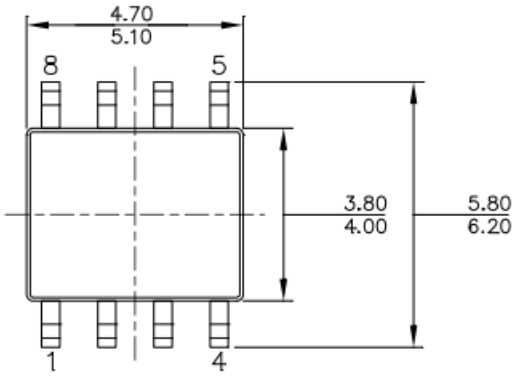
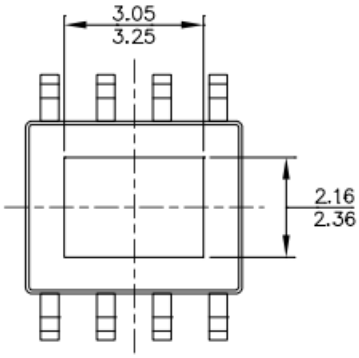


Figure 25. PCB Layout Example

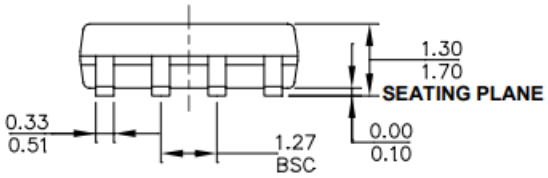
PACKAGE INFORMATION



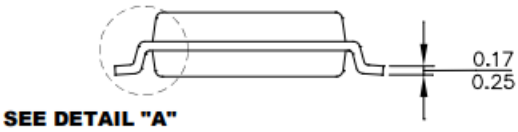
TOP VIEW



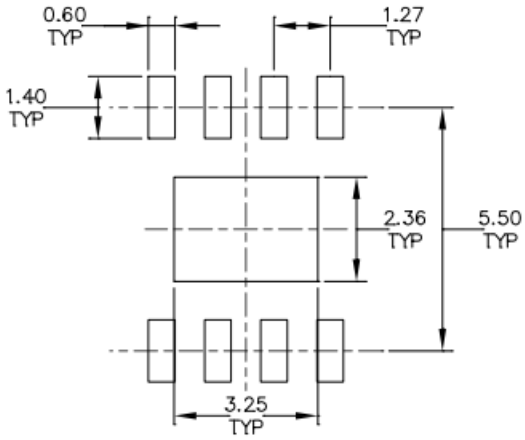
BOTTOM VIEW



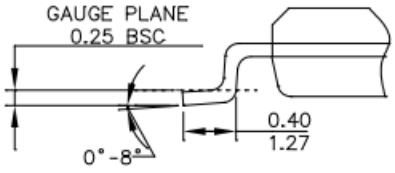
FRONT VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

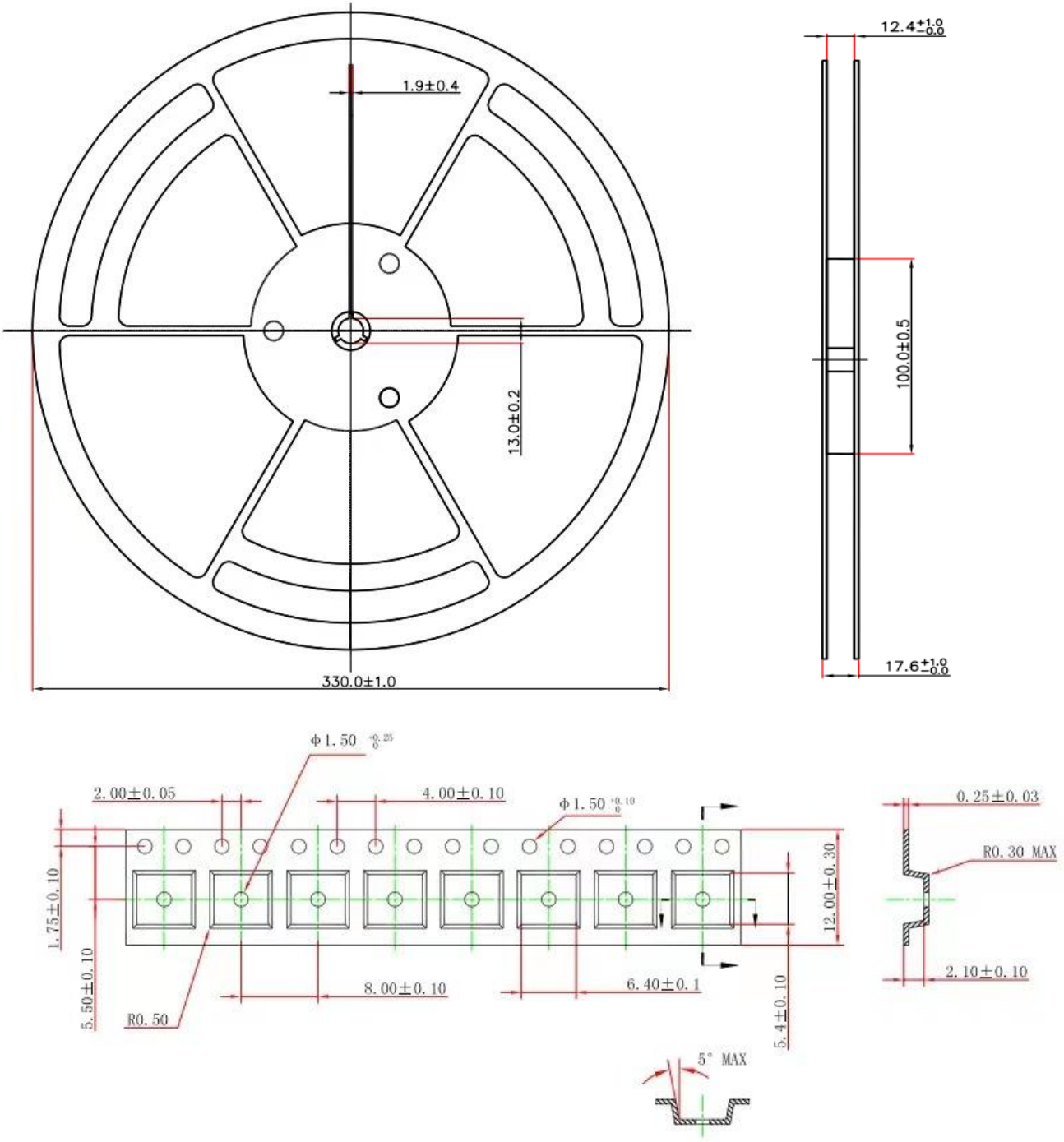


DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING REFERENCE TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

TAPE AND REEL INFORMATION



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