4.5V-100V Vin, 1A, Constant On-Time Synchronous BUCK Converter

FEATURES

- Wide Input Range: 4.5V-100V
- 1A Continuous Output Current
- Integrated 530mΩ High-Side and 220mΩ Low-Side Power MOSFETs
- 150uA Quiescent Current
- 1.2V ±1% Feedback Reference Voltage at Room Temperature
- 4.3ms Internal Soft-start Time
- Programmable Switching Frequency Range 100KHz ~ 600KHz
- COT Control Mode
- PFM operation mode at light load
- Precision Enable Threshold for Programmable Input UVLO Threshold and Hysteresis
- Cycle-by-Cycle Current Limiting
- Over-Voltage Protection
- Over-Temperature Protection
- Available in an ESOP-8 Package

APPLICATIONS

- 48V Industry Power Bus System
- E-bike, Scooter
- BMS

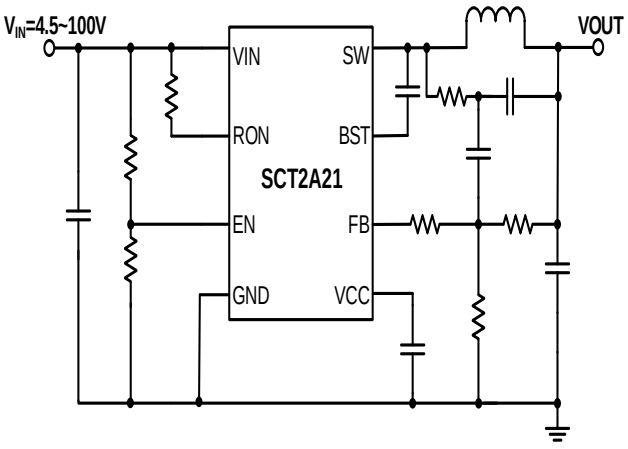
DESCRIPTION

The SCT2A21 is a 1A synchronous buck converters with wide input voltage, ranging from 4.5V to 100V, which integrates an 530mΩ high-side MOSFET and a 220mΩ low-side MOSFET. The SCT2A21, adopting the constant-on time (COT) mode control, supports the PFM mode with typical 150uA low quiescent current which assists the converter on achieving high efficiency at light load or standby condition. Applying an external diode on VCC pin from converter output, the quiescent current can be further reduced.

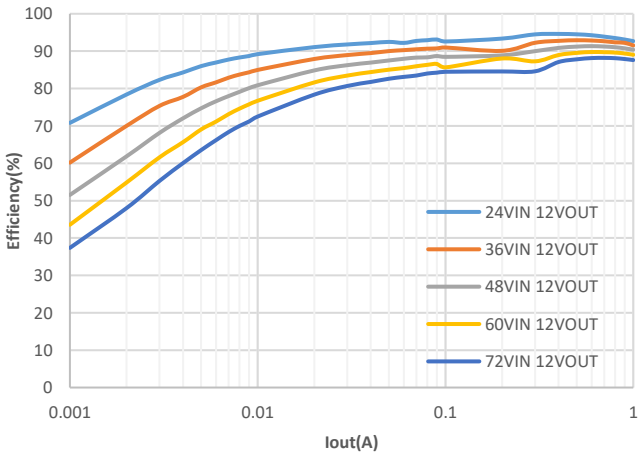
The SCT2A21 features programmable switching frequency from 100 kHz to 600KHz with an external resistor, which provides the flexibility to optimize either efficiency or external component size.

The SCT2A21 offers cycle-by-cycle current limit, thermal shutdown protection, output over-voltage protection and input voltage under-voltage protection. The device is available in an 8-pin thermally enhanced SOP-8 package.

TYPICAL APPLICATION



Synchronous Buck Application Circuit



Efficiency of VOUT=12V

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Released to Market

Revision 1.1: Update DEVICE ORDER INFORMATION.

DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT2A21STER	Tape & Reel	4000	2A21	8	ESOP-8

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN, EN, RON	-0.3	105	V
BOOT	-0.3	110	V
SW	-1	105	V
VCC	-0.3	30	V
BOOT-SW	-0.3	6	V
FB	-0.3	6	V
Operating junction temperature T_J(2)	-40	150	°C
Storage temperature TSTG	-65	150	°C

PIN CONFIGURATION

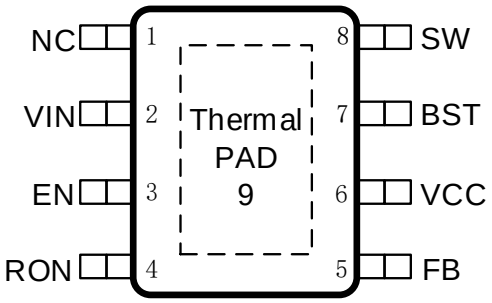


Figure 1. 8-Lead Plastic E-SOP8

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
NC	1	No Connection
VIN	2	Input supply voltage. Connect a local bypass capacitor from VIN pin to GND pin. Path from VIN pin to high frequency bypass capacitor and GND must be as short as possible.
EN	3	Enable pin to the regulator with internal pull-up current source. a) Float or connect to VIN or higher than 1.23V to enable the converter. b) Pull below 1.22V to disable the converter. c) Resistor divider from VIN to GND connecting EN pin can adjust the input voltage lockout threshold.
RON	4	On-time programming pin. A resistor between this pin and VIN sets the switch ON time.
FB	5	Inverting input of the internal PWM comparator. The tap of external feedback resistor divider from the output to GND sets the output voltage. The device regulates FB voltage to the internal reference value of 1.2V typical.
VCC	6	Output from the Internal High Voltage Regulator. The internal VCC regulator provides bias supply for the gate drivers and other internal circuitry. A larger than 1.0μF decoupling capacitor is needed, recommended 2.2μF.

BST	7	Power supply bias for high-side power MOSFET gate driver. Connect a 0.1uF capacitor from BOOT pin to SW pin. Bootstrap capacitor is charged when low-side power MOSFET is on or SW voltage is low.
SW	8	Regulator switching output. Connect SW to an external power inductor
Thermal Pad	9	Heat dissipation path of die and also is GND PIN. Must be connected to ground plane on PCB for proper operation and optimized thermal performance.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	4.5	100	V
V_{CC}	External V_{CC} bias voltage	7.5	30	V
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-1	+1	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins(2)	-1	+1	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	ESOP-8L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	41.1	°C/W
$R_{\theta JC}$	Junction to case thermal resistance(1)	37.3	
$R_{\theta JB}$	Junction to board thermal resistance	30.6	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2A21 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT2A21. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

ELECTRICAL CHARACTERISTICS

V_{IN}=48V, T_J=-40°C~125°C, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Operating input voltage		4.5		100	V
V_{CC}	V_{CC} Regulator Output			7.3		V
V_{CC_UVLO}	V_{CC} UVLO Threshold	V_{IN} rising		4.1	4.48	V
	Hysteresis			220		mV
I_{VCC_LIM}	V_{CC} internal LDO current limit	VCC short to ground		30		mA
I_{SHDN}	Shutdown current from VIN pin	EN=0, no load		3	8	μA
I_Q	Quiescent current from VIN pin	EN floating, no load, non-switching, BOOT-SW=5V		150	250	μA
Power MOSFETs						
R_{DSON_H}	High-side MOSFET on-resistance	V_{BOOT}-V_{SW}=5V		530	950	mΩ
R_{DSON_L}	Low-side MOSFET on-resistance			220	450	mΩ
Reference and Control Loop						
V_{REF}	Reference voltage of FB	T_J=25°C	1.188	1.2	1.212	V
		T_J=-40°C~125°C	1.178	1.2	1.222	V
Enable and Soft-startup						
V_{EN_H}	Enable high threshold			1.23		V
V_{EN_L}	Enable low threshold			1.22		V
V_{EN_HYS}	Enable hysteresis threshold			10		mV
I_{EN_L}	Enable pin pull-up current	EN=1V		0.35		μA
I_{EN_H}	Enable pin pull-up current	EN=1.5V		17.8		μA
T_{SS}	Internal soft start current			4.3		ms
Switching Frequency Timing						
T_{ON}	ON time	V_{IN}=24V, R_{ON}=100k		420		ns
T_{OFF_MIN}	Minimum off-time	V_{IN}=12V		200	260	ns
Current Limit and Over Current Protection						
I_{LIM_HS}	HS MOSFET current limit	From drain to source	1.25	1.5	1.8	A
I_{LIM_LS}	LS MOSFET current limit	From source to drain		1.1		A
Izc	LS zerocross current limit	From source to drain for PSM mode		75		mA
I_{LIM_LSROC}	LS reverse current limit	From drain to source protection		3.5		A
Protection						
V_{OVP}	Feedback overvoltage with respect to reference voltage	V_{FB}/V_{REF} rising		120		%
		V_{FB}/V_{REF} falling		115		%
V_{UVP}	Feedback undervoltage with respect to reference voltage	V_{FB}/V_{REF} rising		80		%
		V_{FB}/V_{REF} falling		75		%
T_{SD}	Thermal shutdown threshold*	T_J rising		173		°C
		Hysteresis		25		°C

*Derived from bench characterization

TYPICAL CHARACTERISTICS

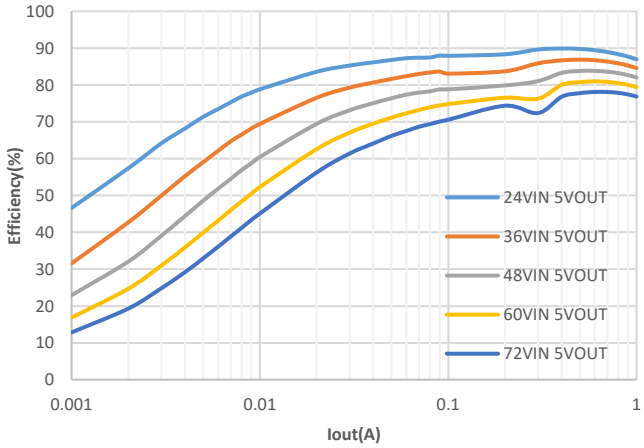


Figure 2. Efficiency, Fsw=300k, Vout=5V

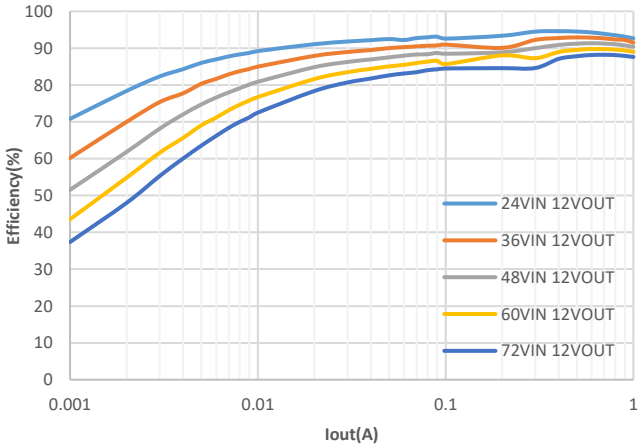


Figure 3. Efficiency, Fsw=300k, Vout=12V

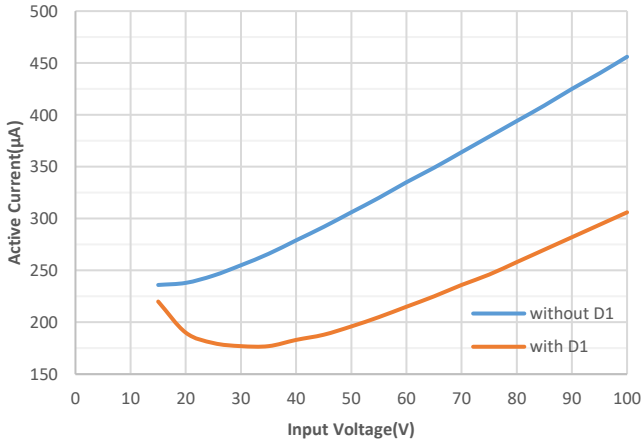


Figure 4. Vin Active Current vs Input Voltage, Vout=12V

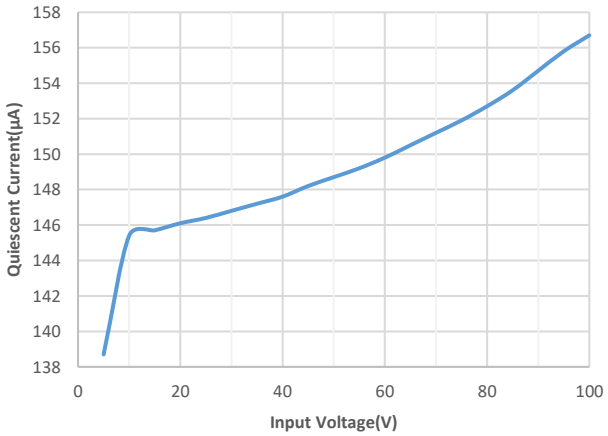


Figure 5. I_Q vs Input Voltage

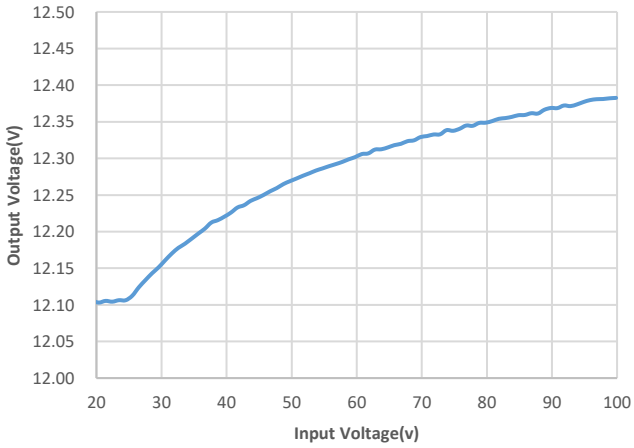


Figure 6. Line Regulation, Vout=12V, Iload=0.5A

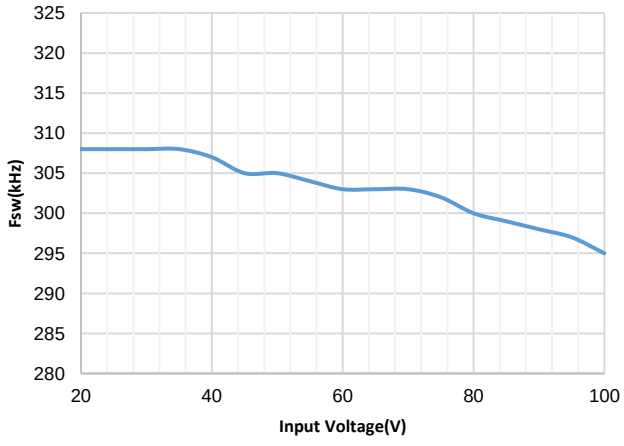


Figure 7. Fsw VS Vin, Vout=12V, Ron=400K

FUNCTIONAL BLOCK DIAGRAM

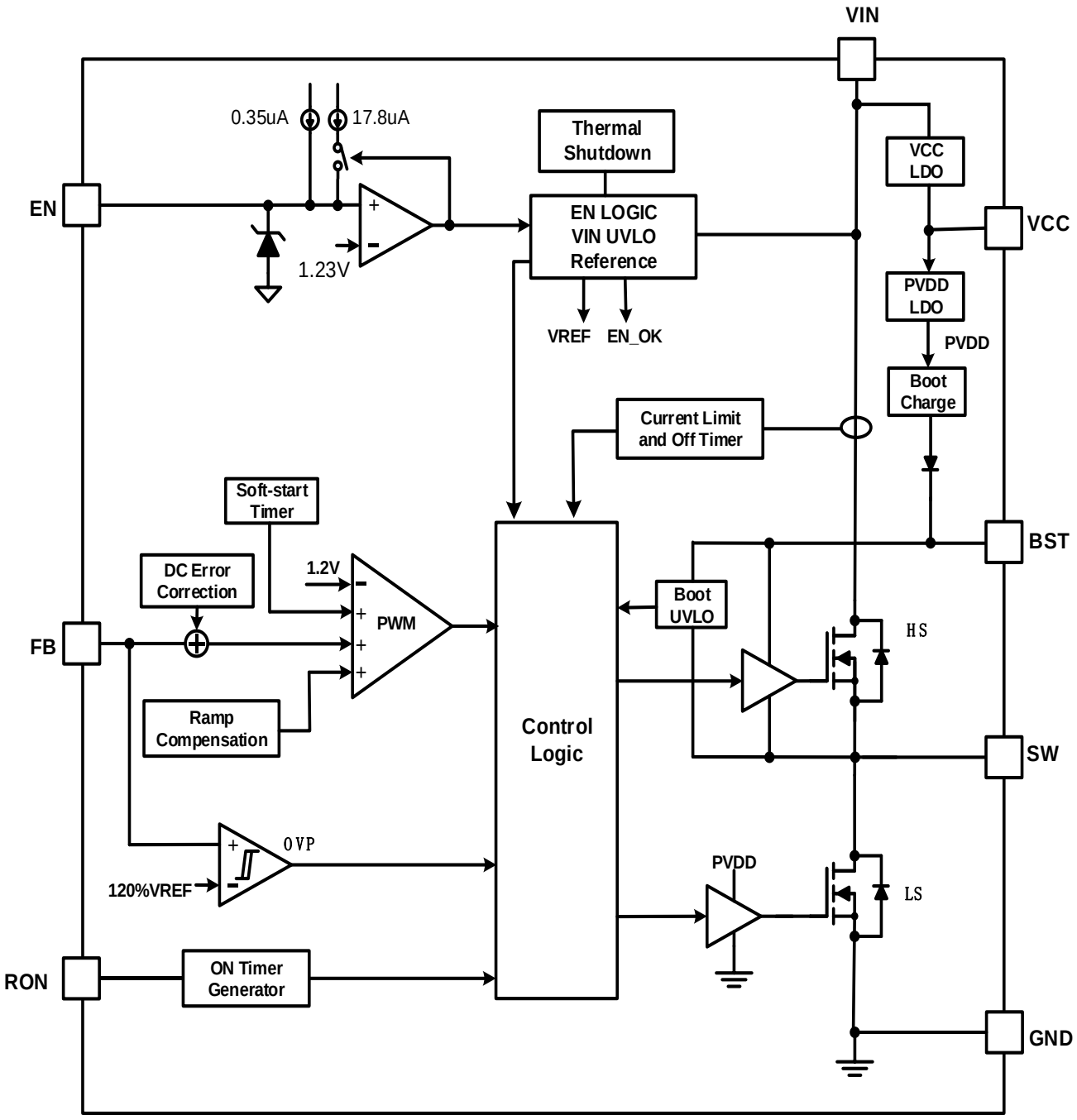


Figure 8. Functional Block Diagram

OPERATION

Overview

The SCT2A21 is a 4.5V-100V input, 1A output, synchronous buck converter with built-in 530mΩ high-side and 220mΩ low-side power MOSFETs. It implements constant on time control to regulate output voltage, providing excellent line and load transient response.

The device operates in Pulse Frequency Modulation (PFM) mode at light loading to provides high light load efficiency. The quiescent current is typically 150uA under no load or sleep mode condition to achieve high efficiency at light load. Applying an external diode on VCC pin from converter output, the quiescent current can be further reduced.

The SCT2A21 features an internal 4.3ms soft-start time to avoid large inrush current and output voltage overshoot during startup. The switching frequency is programmed by the resistor from V_{IN} pin to R_{ON} pin.

The SCT2A21 has a default input start-up voltage of 4.1V with 220mV hysteresis. The EN pin is a high-voltage pin with a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher UVLO system requirements. Floating EN pin enables the device with the internal pull-up current to the pin. Connecting EN pin to VIN directly starts up the device automatically.

The SCT2A21 full protection features include the input under-voltage lockout, the output over-voltage protection, over current protection with cycle-by-cycle current limiting, output hard short protection and thermal shutdown protection.

Constant On-Time Mode Control

The SCT2A21 employs constant on-time (COT) Mode control providing fast transient with pseudo fixed switching frequency. At the beginning of each switching cycle, since the feedback voltage (VFB) is lower than the internal reference voltage (VREF), the high-side MOSFET (Q1) is turned on during one on-time and the inductor current rises to charge up the output voltage. The on-time is determined by the input voltage and Ron resistor. After the on-time, the Q1 turns off and the low-side MOSFET (Q2) turns on after dead time duration. The inductor current drops and the output capacitors are discharged. When the output voltage decreases and the VFB decreased below the VREF, the Q1 turns on during one on-time after another dead time duration. This repeats on cycle-by-cycle based.

The on time of the SCT2A21 is determined by the R_{ON} resistor and is inversely proportional to the input voltage. The inverse relationship with V_{IN} results in a nearly constant frequency as V_{IN} is varied. The On time can be calculated from Equation 1.

$$T_{ON} = \frac{1 \times 10^{-10} \times R_{ON}}{V_{IN}} \quad (1)$$

To set a specific continuous conduction mode switching frequency, the R_{ON} resistor is determined by Equation 2:

$$R_{ON} = \frac{V_{OUT}}{1 \times 10^{-10} \times F_{SW}} \quad (2)$$

R_{ON} must be selected for a minimum on-time (at maximum VIN) greater than 150 ns for proper operation.

Current limit

The inductor current is monitored during high-side MOSFET turn on. The SCT2A21 implements over current protection with cycle-by-cycle limiting high-side MOSFET peak current during unexpected overload or output hard short condition.

SCT2A21 also provide a HS current limit off timer for making the IC safer when trigger over current condition. Once trigger HS over current, the present on-time period is immediately terminated, and will force LS turn on a non-resettable off timer for avoiding the inductor current run away. The length of off time is controlled by FB voltage and VIN voltage and could be calculated by the following equation.

$$T_{off} = 1.5 * \left(\frac{V_{IN}}{20 * V_{FB} + 4.35}\right) us \quad (3)$$

Ripple Injection

SCT2A21 adopts Constant-On-Time (COT) control in which the on-time is terminated by an on-timer and the off-time is terminated by the feedback voltage (VFB) falling below the reference voltage (VREF). Therefore, for stable operation, the feedback voltage must decrease monotonically, in phase with the inductor current during the off time. Furthermore, this change in feedback voltage (VFB) during off-time must be larger than any noise component present at the feedback node. A type 3 ripple injection configuration is recommended for minimum output ripple.

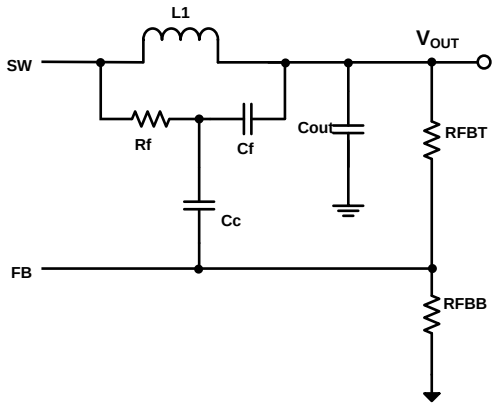


Figure 9. Ripple Injection Network

The ripple injection network applies an RC filter (R_f and C_f) across SW and VOUT to generate a triangular ramp that is in phase with the inductor current. Then this triangular ramp is coupled into the feedback node via capacitor C_C. RC filter value is calculated as Equation 4 to provide the required ripple amplitude at the FB pin..

$$R_f C_f \leq \frac{(V_{IN} - V_{OUT}) \times t_{ON}}{V_{ripple}} \quad (4)$$

Where

- F_{SW} is switching frequency
- R_{FBT} Top feedback resistor; R_{FBB} Bottom feedback resistor
- V_{ripple} is ripple voltage injected to FB pin, 25mV is recommended

C_C value should be chosen to avoids excessive coupling capacitor discharge by the feedback resistors during sleep intervals when operating at light loads. Use Equation 6 to calculate C_C value.

$$C_C \geq \frac{t_{settle}}{3 \times R_{FBT}} \quad (5)$$

Where

- t_{settle} desired load transient response settle time
- R_{FBT} Top feedback resistor

VCC Regulator

The SCT2A21 contains an internal high voltage linear regulator with a nominal output voltage of 7.3 V. This regulator supplies power to internal circuit blocks including the synchronous FET gate driver and the logic circuits. An external capacitor at the VCC pin stabilizes the regulator and supplies transient VCC current to the gate drivers. An internal diode connected from VCC to the BST pin replenishes the charge in the high-side gate drive bootstrap capacitor when the SW pin is low.

In high input voltage applications, the power dissipated in the regulator is significant and can limit the efficiency and maximum achievable output power. The SCT2A21 allows the internal VCC regulator power loss to be reduced by supplying the VCC voltage via a diode from an external voltage. The external VCC bias can be supplied from the

SCT2A21 converter output rail if the regulation voltage. When the VCC pin of the SCT2A21 is raised above the regulation voltage (7.3V typical), the internal regulator is disabled and the power dissipation in the IC is reduced.

Enable and Under Voltage Lockout Threshold

The SCT2A21 is enabled when the VIN pin voltage rises about 4.1V and the EN pin voltage exceeds the enable threshold of 1.23V. The device is disabled when the VIN pin voltage falls below 3.88V or when the EN pin voltage is below 1.22V. An internal 0.35uA pull up current source to EN pin allows the device enable when EN pin floats.

EN pin is a high voltage pin that can be connected to VIN directly to start up the device.

For a higher system UVLO threshold, connect an external resistor divider (R3 and R4) shown in Figure 10 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 6 and Equation 7 respectively.

$$VIN\_rise = VEN * \frac{R3 + R4}{R4} \quad (6)$$

$$VIN\_hys = I2 * R3 \quad (7)$$

Where

VIN_rise: Vin rise threshold to enable the device

VIN_hys: Vin hysteresis threshold

I_1=0.35uA: neglect in calculation

I_2=17.8uA

V_{EN}=1.23V, assume VEN_r = VEN_f =1.23V

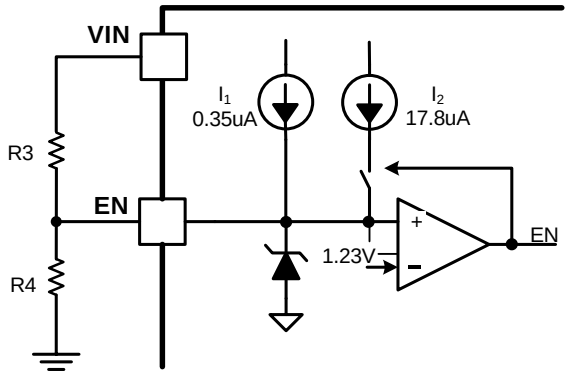


Figure 10. System UVLO by enable divide

Output Voltage

The SCT2A21 regulates the internal reference voltage at 1.2V with ±1% tolerance at room temperature. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 8 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

$$R_{FB\_TOP} = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_{FB\_BOT} \quad (8)$$

where

- R_{FB_TOP} is the resistor connecting the output to the FB pin.
- R_{FB_BOT} is the resistor connecting the FB pin to the ground.

Internal Soft-Start

The SCT2A21 integrates an internal soft-start circuit that ramps the reference voltage from zero volts to 1.2V reference voltage in 4.3ms. If the EN pin is pulled below 1.22V, switching stops and the internal soft-start resets. The soft-start also resets during shutdown due to thermal overloading.

Bootstrap Voltage Regulator

An external bootstrap capacitor between BOOT pin and SW pin powers the floating gate driver to high-side power MOSFET. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

Over voltage Protection

The SCT2A21 implements the Over-Voltage Protection OVP circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. The overvoltage comparator in OVP circuit compares the FB pin voltage to the internal reference voltage. When FB voltage exceeds 120% of internal 1.2V reference voltage, the high-side MOSFET turns off to avoid output voltage continue to increase. When the FB pin voltage falls below 115% of the 1.2V reference voltage, the high-side MOSFET can turn on again.

Thermal Shutdown

The SCT2A21 protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 173C, the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 148C, the device restarts with internal soft start phase.

APPLICATION INFORMATION

Typical Synchronous Buck Application

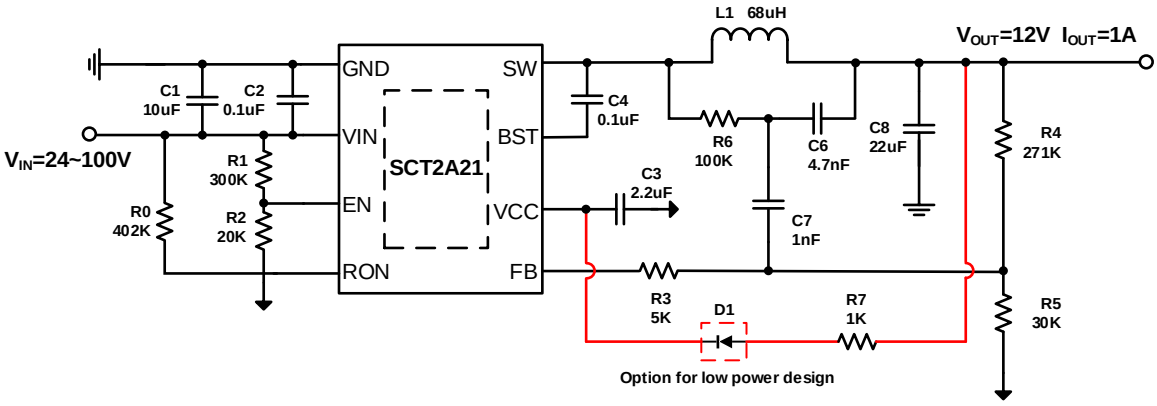


Figure 11. SCT2A21 Design Example, 12V Output with Programmable UVLO

Design Parameters

Design Parameters	Example Value
Input Voltage	48V Normal， 24V to 100V
Output Voltage	12V
Maximum Output Current	1A
Switching Frequency	300 KHz
Output voltage ripple (peak to peak)	30mV
Transient Response 0.1A to 0.9A load step	ΔVout = 210mV

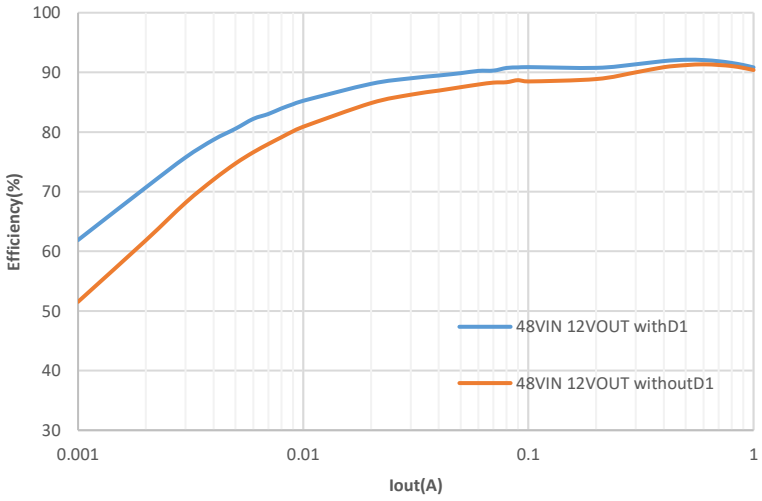


Figure 12 Efficiency, Fsw=300k, Vout=12V with D1 vs without D1

Output Voltage

The output voltage is set by an external resistor divider R4 and R5 in typical application schematic. Recommended R5 resistance is 30KΩ. Use equation 9 to calculate R4.

$$R_4 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_5 \quad (9)$$

where:

- V_{REF} is the feedback reference voltage of 1.2V

Table 1. R_1, R_2Value for Common Output Voltage (Room Temperature)

V_{OUT}	R_4	R_5
5 V	95 KΩ	30 KΩ
12V	271 KΩ	30 KΩ
24V	576 KΩ	30 KΩ

Under Voltage Lock-Out

An external voltage divider network of R_3 from the input to EN pin and R_4 from EN pin to the ground can set the input voltage's Under Voltage Lock-Out (UVLO) threshold. The UVLO has two thresholds, one for power up when the input voltage is rising and the other for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 19.68V (start or enable). After the regulator starts switching, it should continue to do so until the input voltage falls below 14.34V (stop or disable). Use Equation 10 and Equation 11 to calculate the values 300 kΩ and 20 kΩ of R_1 and R_2 resistors.

$$VIN_{rise} = V_{EN\_H} * \frac{R1 + R2}{R2} \quad (10)$$

$$VIN\_hys = I2 * R1 \quad (11)$$

Where

VIN_rise: Vin rise threshold to enable the device

VIN_hys: Vin hysteresis threshold

I2=17.8uA

V_{EN_H}=1.23V

Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance(DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 20%~40% of the maximum output current.

The peak-to-peak ripple current in the inductor I_{LPP} can be calculated as in Equation 12.

$$I_{LPP} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{V_{IN} * L * f_{SW}} \quad (12)$$

Where

- I_{LPP} is the inductor peak-to-peak current
- L is the inductance of inductor
- f_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 13 to calculate the inductance value.

$$L_{MIN} = \frac{V_{OUT}}{f_{SW} * LIR * I_{OUT(max)}} * (1 - \frac{V_{OUT}}{V_{IN(max)}}) \quad (13)$$

Where

- L_{MIN} is the minimum inductance required
- f_{sw} is the switching frequency
- V_{OUT} is the output voltage
- $V_{IN(max)}$ is the maximum input voltage
- $I_{OUT(max)}$ is the maximum DC load current
- LIR is coefficient of I_{LPP} to I_{OUT}

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in equation 14 and equation 15.

$$I_{LPEAK} = I_{OUT} + \frac{I_{LPP}}{2} \quad (14)$$

$$I_{LRMS} = \sqrt{(I_{OUT})^2 + \frac{1}{12} * (I_{LPP})^2} \quad (15)$$

Where

- I_{LPEAK} is the inductor peak current
- I_{OUT} is the DC load current
- I_{LPP} is the inductor peak-to-peak current
- I_{LRMS} is the inductor RMS current

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 1.5A. The most conservative approach is to choose an inductor with a saturation current rating greater than 1.5A. Because of the maximum I_{LPEAK} limited by device, the maximum output current that the SCT2A21 can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a lower maximum output current.

Input Capacitor Selection

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g. 0.1uF) with small package size (0603) to filter high frequency switching noise. Place the small size capacitor as close to VIN and GND pins as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input capacitor can be calculated using Equation 16.

$$I_{CINRMS} = I_{OUT} * \sqrt{\frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})} \quad (16)$$

The worst case condition occurs at V_{IN}=2*V_{OUT}, where:

$$I_{CINRMS} = 0.5 * I_{OUT} \quad (17)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increasing.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 18 and the maximum input voltage ripple occurs at 50% duty cycle.

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} * C_{IN}} * \frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}}) \quad (18)$$

For this example, one 10μF, X7R ceramic capacitors rated for 100 V in parallel are used. And a 0.1 μF for high-frequency filtering capacitor is placed as close as possible to the device pins.

Bootstrap Capacitor Selection

A 0.1μF ceramic capacitor must be connected between BOOT pin and SW pin for proper operation. A ceramic capacitor with X7R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 19 desired.

$$\Delta V_{OUT} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{8 * {f_{SW}}^2 * L * C_{OUT} * V_{IN}} \quad (19)$$

Where

- $\Delta V_{OUT}$is the output voltage ripple
- f_{SW} is the switching frequency
- L is the inductance of inductor
- C_{OUT} is the output capacitance
- V_{OUT} is the output voltage
- $V_{IN}$is the input voltage

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, one 22μF ceramic output capacitors work for most applications.

Table 2 and Table 3 lists typical values of external components for some standard output voltages.

Table 2: Component List with Typical Output Voltage BOM list (Fsw=300KHz)

Vout	L1	COUT	R0	R4	R5	R6	C6	C7
5V	33uH	22uF	165K	95K	30K	100K	3.3nF	1nF
12V	68uH	22uF	402K	271K	30K	100K	4.7nF	1nF
24V	100uH	22uF	806K	576k	30K	100k	6.8nF	1nF

Table 3: Component List with Typical Output Voltage BOM list (Fsw=600KHz)

Vout	L1	COUT	R0	R4	R5	R6	C6	C7
5V	15uH	22uF	82.5K	95K	30K	80.6K	1.5nF	1nF
12V	33uH	22uF	200K	271K	30K	100K	2.2nF	1nF
24V	56uH	22uF	402K	576k	30K	100k	3.3nF	1nF

Application Waveforms

Vin=48V, Vout=12V, Fsw=300k, unless otherwise noted

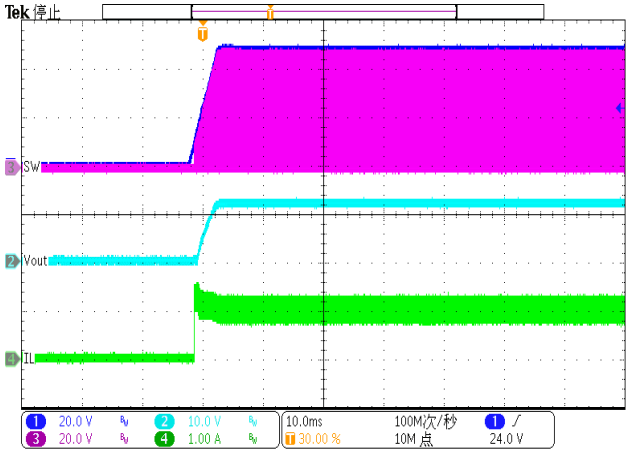


Figure 13. Power up (Iload=1A)

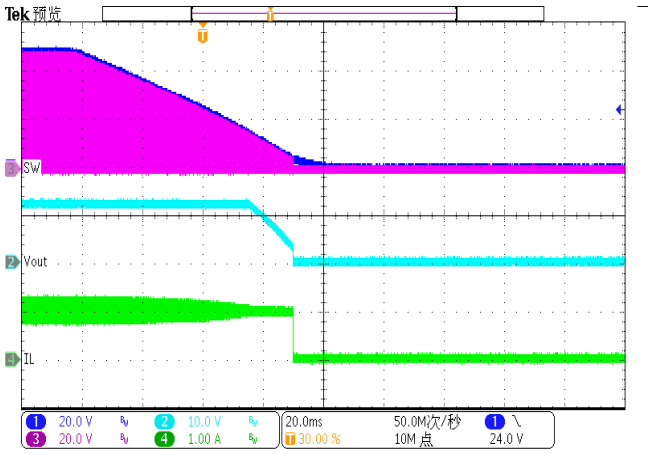


Figure 14. Power down (Iload=1A)

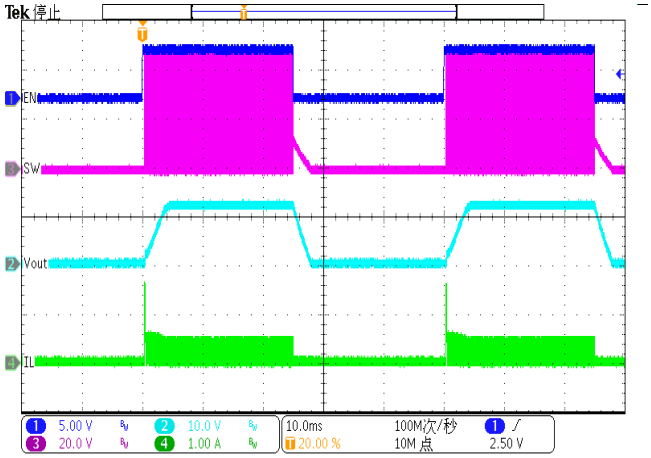


Figure 15. Enable toggle (Iload=0.1A)

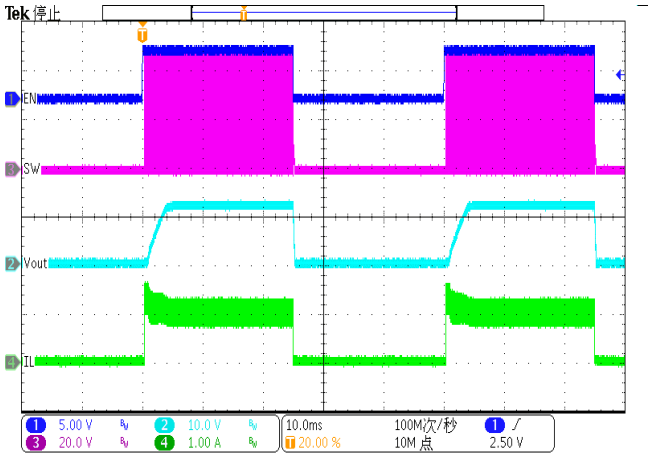


Figure 16. Enable toggle (Iload=1A)

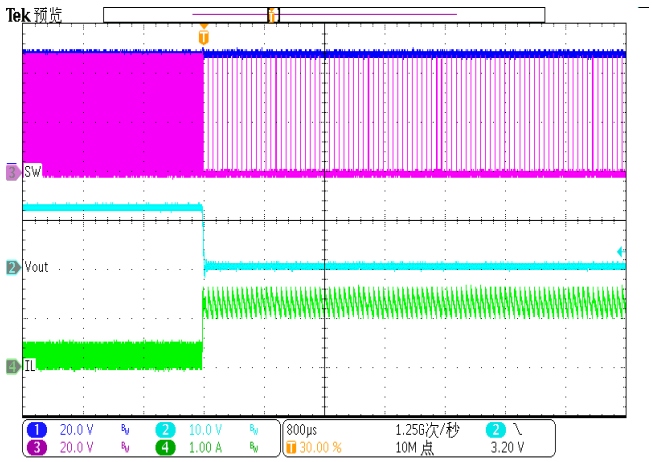


Figure 17. Output Hard Short

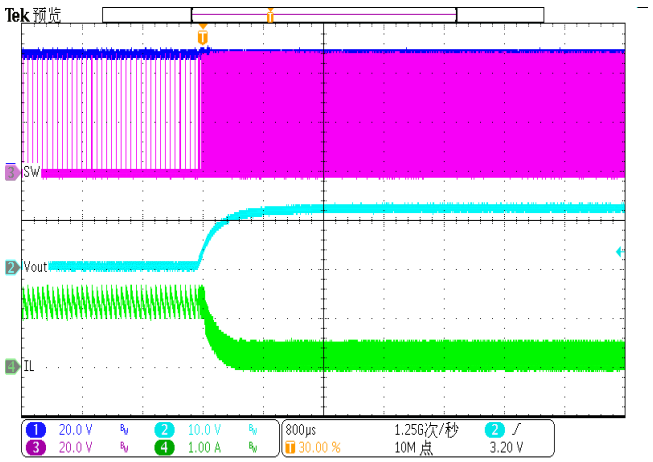


Figure 18. Output Hard Short Release

Application Waveforms (Continued)

Vin=48V, Vout=12V, Fsw=300k, unless otherwise noted

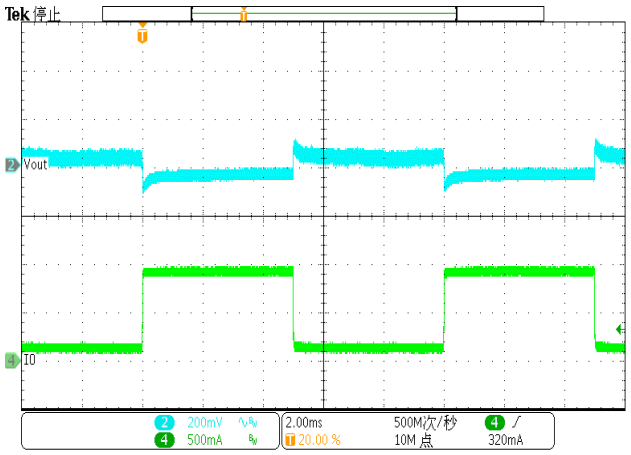


Figure 19. Load Transient (0.1A to 0.9A, 1.6A/us)

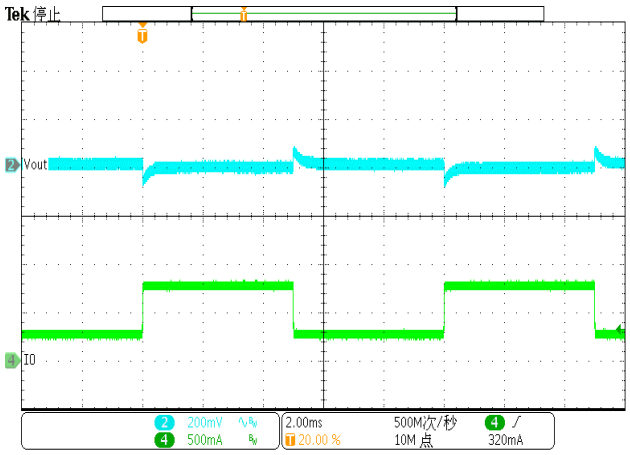


Figure 20. Load Transient (0.25A to 0.75A, 1.6A/us)

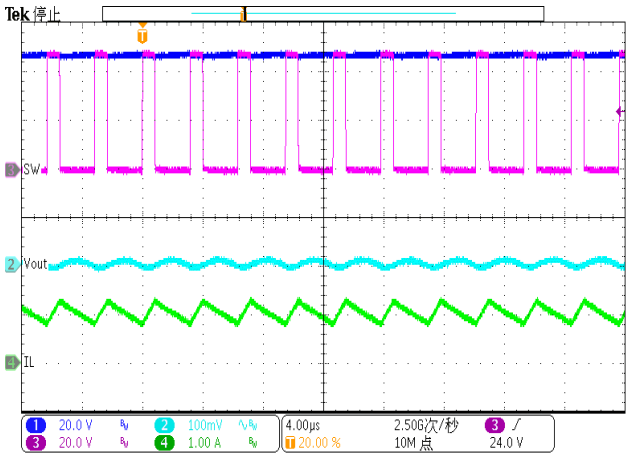


Figure 21. Output Ripple (Iload=1A)

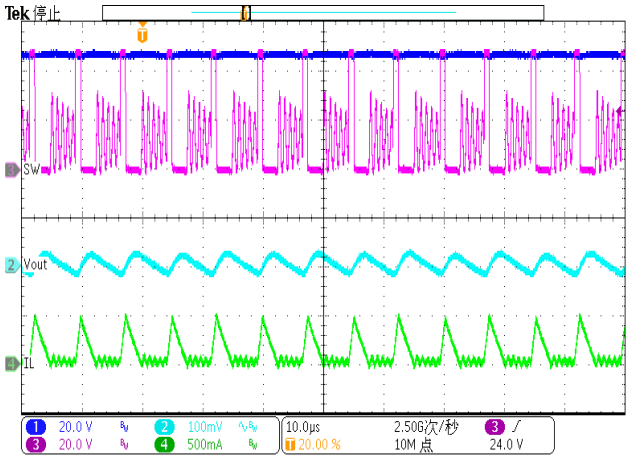


Figure 22. Output Ripple (Iload=0.1A)

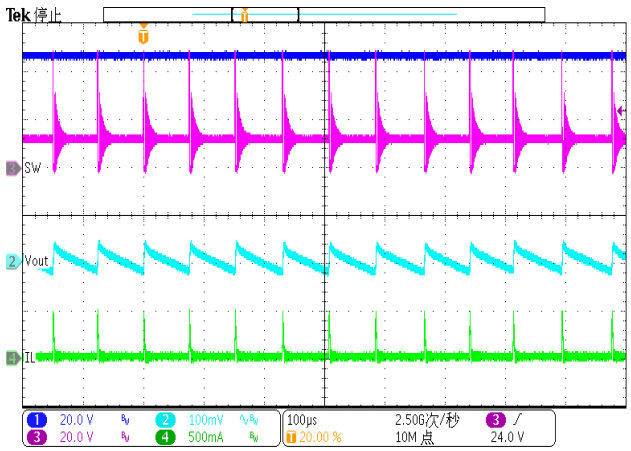


Figure 23. Output Ripple (Iload=0.01A)

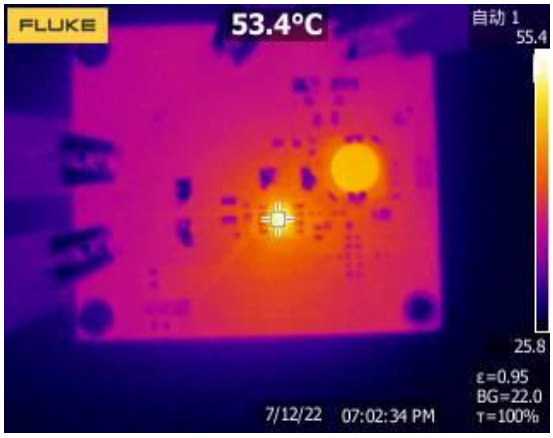
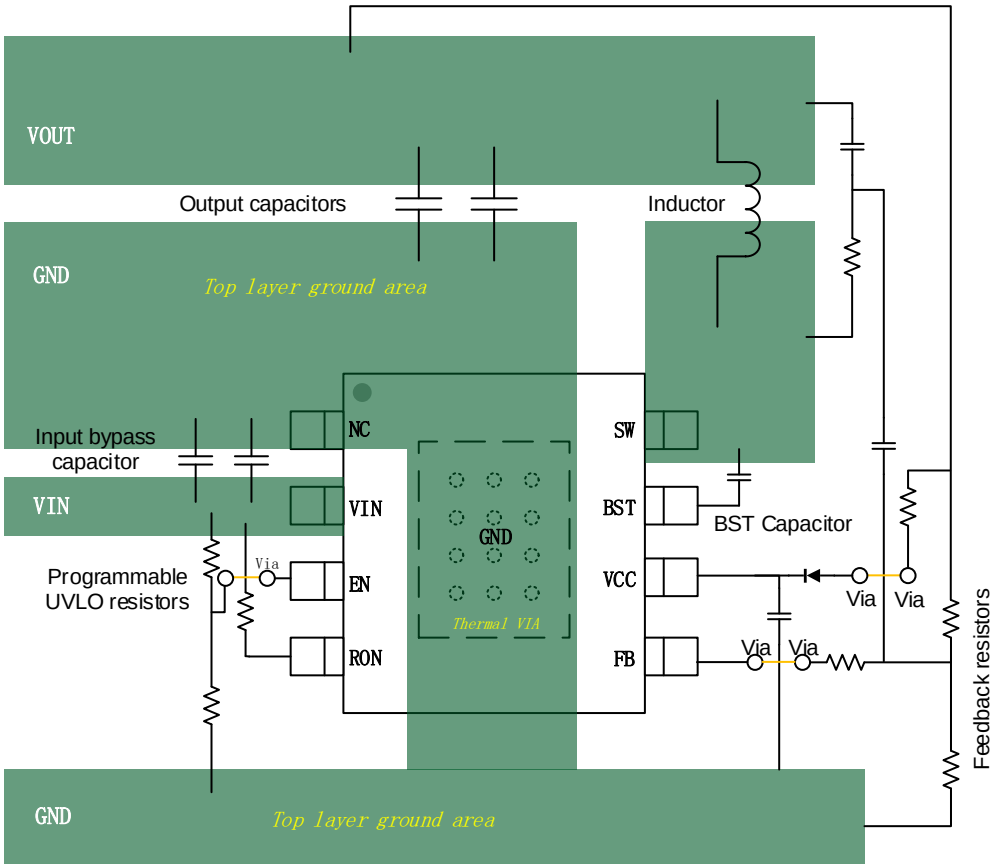


Figure 24. Thermal, 48VIN, 12Vout, 1A

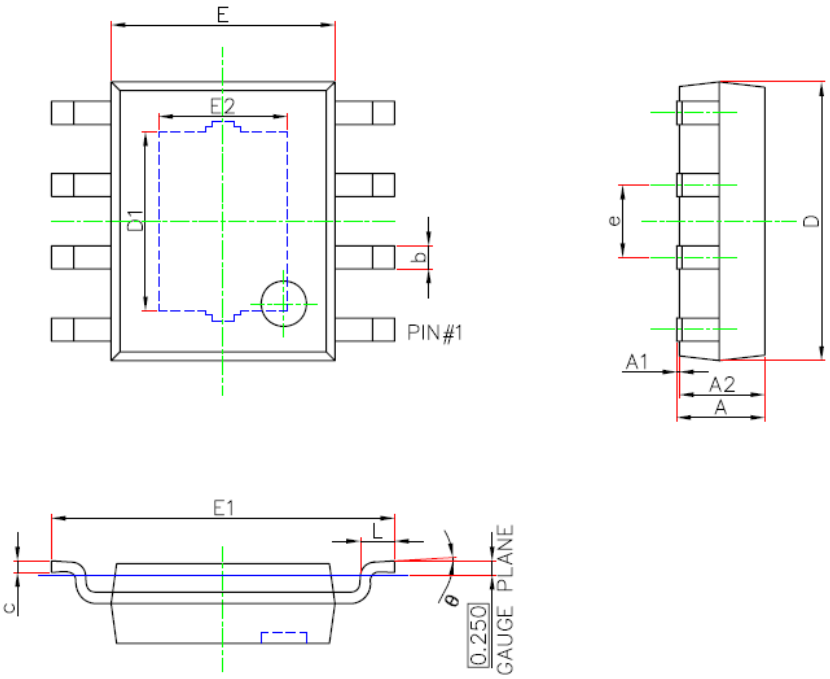
Layout Guideline

Proper PCB layout is a critical for SCT2A21's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.
2. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
3. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.
4. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground planes using multiple vias directly under the IC. The center thermal pad should always be soldered to the board for mechanical strength and reliability, using multiple thermal vias underneath the thermal pad. Improper soldering thermal pad to ground plate on PCB will cause SW higher ringing and overshoot besides downgrading thermal performance. It is recommended 8mil diameter drill holes of thermal vias, but a smaller via offers less risk of solder volume loss. On applications where solder volume loss thru the vias is of concern, plugging or tenting can be used to achieve a repeatable process.
5. Output inductor should be placed close to the SW pin. The area of the PCB conductor minimized to prevent excessive capacitive coupling.
6. UVLO adjust, VCC capacitor and feedback components should connect to small signal ground which must return to the GND pin without any interleaving with power ground.
7. For achieving better thermal performance, a four-layer layout is strongly recommended.



PACKAGE INFORMATION



ESOP8(95x130) Package Outline Dimensions

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.300	1.700	0.051	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	3.050	3.250	0.120	0.128
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.160	2.360	0.085	0.093
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

TAPE AND REEL INFORMATION