20V Output, 16A Switching Current, Fully Integrated Synchronous Boost Converter with Programmable Peak Current Limit

FEATURES

- Wide Input Voltage Range: 2.7V-20V
- Wide Output Voltage Range: 4.5V-20V
- Fully Integrated 10mΩ High Side FET and 6.5mΩ Low Side FET
- Programmable Peak Current Limit Up to 16A
- Typical Shut-down Current: 5uA
- Quiescent Current: 170uA
- Fixed 600KHz Switching Frequency
- Selectable PFM and FCCM at Light-load
- Parallel Mode
- External Soft Start and Compensation
- Output Overvoltage Protection
- Thermal Shutdown Protection
- QFN-13 3mm x 4mm Package

APPLICATIONS

- Bluetooth Audio
- Wireless Charger
- POS
- Lighting

DESCRIPTION

The SCT12A6 is a high efficiency synchronous boost converter with fully integrated a 10mΩ high-side MOSFET and a 6.5mΩ low-side MOSFET, supporting 2.7V to 20V input voltage range and up to 16A switching current. The peak current limit can be adjustable with an external resistor. SCT12A6 supports up to 30W of load power from a 1-cell battery with integrated low Rds_on power MOSFETs.

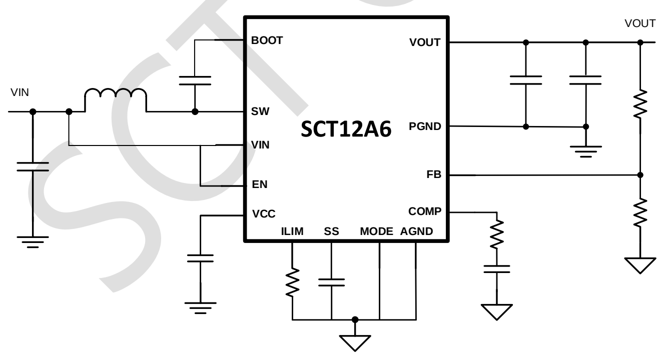
The SCT12A6 adopts constant off-time peak current control to provide fast transient response. An external compensation network allows flexibility setting loop dynamics to achieve optimal transient performance at different load conditions.

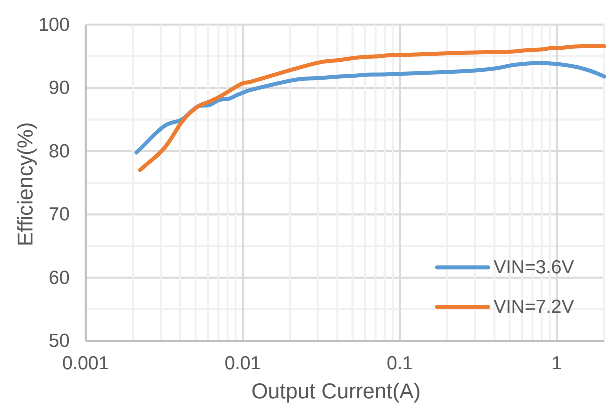
The SCT12A6 offers selectable PFM and FCCM in light load condition, and it also offers parallel mode for higher power application. The switching frequency is fixed 600KHz.

The SCT12A6 features output overvoltage protection and thermal shutdown protection when the device overloads.

The device is available in a QFN-13 3mm x 4mm package.

TYPICAL APPLICATION





Efficiency, V_{OUT}=12V, PFM

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 0.8: Customer Sample.

Revision 0.81: Specification and Description Update.

DEVICE ORDER INFORMATION

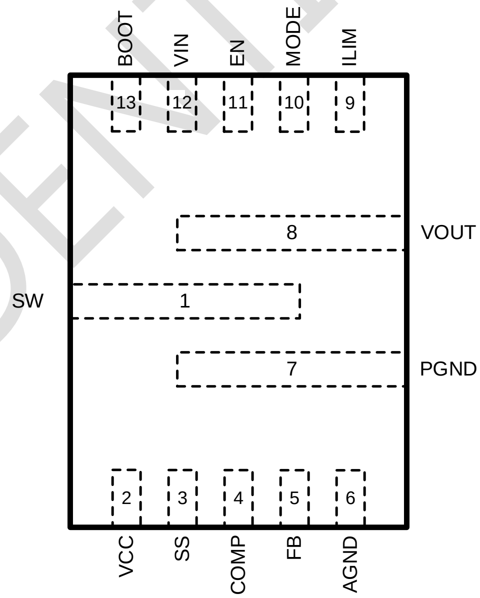
PART NUMBER	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT12A6FOAR	Tape & Reel	5000	12A6	13	QFN-13 3mm×4mm

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
BOOT	-0.3	28	V
VIN, SW, VOUT, EN	-0.3	22	V
VCC, ILIM, FB, COMP, SS, MODE	-0.3	5.5	V
Operating Junction Temperature T_J(2)	-40	125	°C
Storage Temperature T_{STG}	-65	150	°C

PIN CONFIGURATION



Top View: 13-Lead Plastic QFN 3mm x 4mm

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 175°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
SW	1	Switching node of the boost converter.
VCC	2	Internal linear regulator output. Connect a 1uF or larger ceramic capacitor to ground. VCC can not to be externally driven. No additional components or loading is recommended on this pin.
SS	3	Place a ceramic cap from this pin to ground to program soft-start time. An internal 8uA current source pulls SS pin to VCC.
COMP	4	Output of the error amplifier and switching converter loop compensation point.
FB	5	Feedback Input. Connect a resistor divider from VOUT to FB to set up output voltage.
AGND	6	Analog Ground. Connected to PGND with single point.

PGND	7	Power ground. Must be soldered directly to ground planes using multiple vias directly under the IC for improved thermal performance and electrical contact.
VOUT	8	Boost converter output. Connect a 1uF decoupling capacitor as close to VOUT pins and power ground pad as possible to reduce the ringing voltage of SW.
ILIM	9	Inductor peak current limit setting. A resistor connecting this pin to ground sets the peak current limit through low-side power FET.
MODE	10	PFM or FCCM mode selection. Connect the pin to VCC to force the device in Forced Continuous Current Modulation (FCCM) operation mode. Ground the pin to operate the device in Pulse Frequency Modulation (PFM) mode.
EN	11	Enable logic input. Pull low to disable the converter. Pull high or connect to VIN to enable the converter. Do not leave EN pin floating.
VIN	12	Power supply input. Must be locally bypassed with a capacitor as close as possible to the pin.
BOOT	13	Power supply for the high-side power MOSFET gate driver. Must connect a 0.1uF or greater ceramic capacitor between BOOT pin and SW node.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted.

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	2.7	20	V
V_{OUT}	Output voltage range	4.5	20	V
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV
	Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014specification, all pins	-1	+1	kV

(1) Except for SW, BOOT to other pins.

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	QFN-13L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	56.23	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.11	
Ψ_{JB}	Junction-to-board characterization parameter(1)	4.92	
$R_{\theta JCtop}$	Junction to case thermal resistance(1)	27.9	
$R_{\theta JB}$	Junction-to-board thermal resistance(1)	4.85	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT12A6 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT12A6. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

ELECTRICAL CHARACTERISTICS

V_{IN}=3.6V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		2.7		20	V
V_{OUT}	Output voltage range		4.5		20	V
V_{IN_UVLO}	Input UVLO	V_{IN} rising		2.5	2.65	V
	Hysteresis			200		mV
I_{SD}	Shutdown current	EN=0, no load and measured on VIN pin		5		uA
I_Q	Quiescent current from VIN	EN=2V, V_{OUT}=12V, no load, no switching		2	4	uA
	Quiescent current from VOUT			170	220	uA
V_{CC}	Internal linear regulator	I_{VCC}=5mA, V_{IN}=6V		5		V
Reference and Control Loop						
V_{REF}	Reference voltage of FB	T_J=25°C	0.98	1	1.02	V
		T_J=-40~125°C	0.97	1	1.03	
I_{FB}	FB pin leakage current	V_{FB}=1V			100	nA
G_{EA}	Error amplifier trans-conductance	V_{COMP}=1.5V		200		uS
I_{COMP_SRC}	Error amplifier maximum source current	V_{FB}=V_{REF}-200mV, V_{COMP}=1.5V		20		uA
I_{COMP_SNK}	Error amplifier maximum sink current	V_{FB}=V_{REF}+200mV, V_{COMP}=1.5V		20		uA
V_{COMP_H}	COMP high clamp	V_{FB}=0.8V, R_{ILIM}=150kΩ		1.3		V
V_{COMP_L}	COMP low clamp	V_{FB}=1.2V, R_{ILIM}=150kΩ		0.9		V
Power MOSFETs						
R_{DSON_H}	High side FET on-resistance			10	19	mΩ
R_{DSON_L}	Low side FET on-resistance			6.5	13	mΩ
Current Limit						
I_{LIM}	Peak current limit	R_{ILIM}=150kΩ		10		A
Enable						
V_{EN}	Enable high threshold (switching)	V_{CC}=5V		1.25		V
	Enable high threshold (internal circuit)				1.0	V
	Enable low threshold (internal circuit)		0.4			V
I_{EN}	Enable hysteresis current	V_{EN}=1.1V		5		uA
I_{SS}	Soft-start Current		6	8	10	uA
MODE Selection						
V_{MD_PWM}	PWM mode with logic high threshold	V_{CC}=5V	4.15			V
V_{MD_PFM}	PFM mode input logic low threshold				0.7	V
Switching Frequency						
F_{SW}	Switching frequency	V_{OUT}=12V, no load, FCCM	540	600	660	kHz
t_{ON_MIN}	Minimum on-time	V_{OUT}=12V		180		ns
Protection						
V_{OVP_VOUT}	Output overvoltage threshold	V_{OUT} rising		22		V

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
	Hysteresis			400		mV
T_{SD}(1)	Thermal shutdown threshold	T_J rising		175		°C
	Hysteresis			25		°C

(1) Guaranteed by sample characterization, not tested in production.

TYPICAL CHARACTERISTICS

V_{IN}=3.6V, V_{OUT}=12V, unless otherwise noted

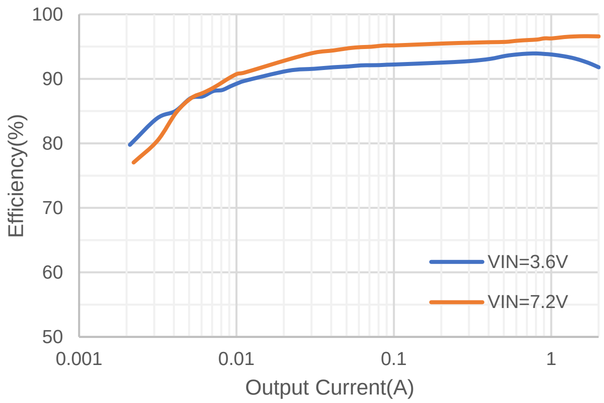


Figure 1. Efficiency, PFM

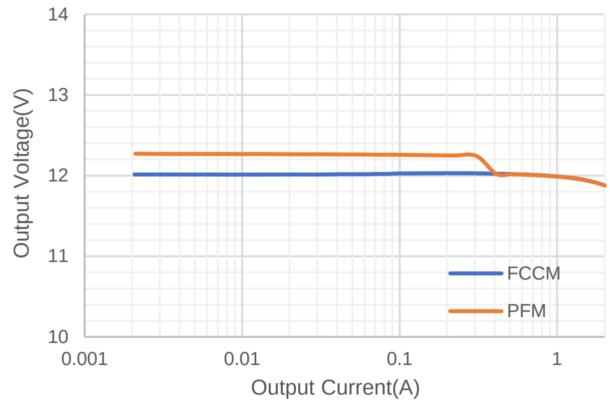


Figure 2. Load Regulation

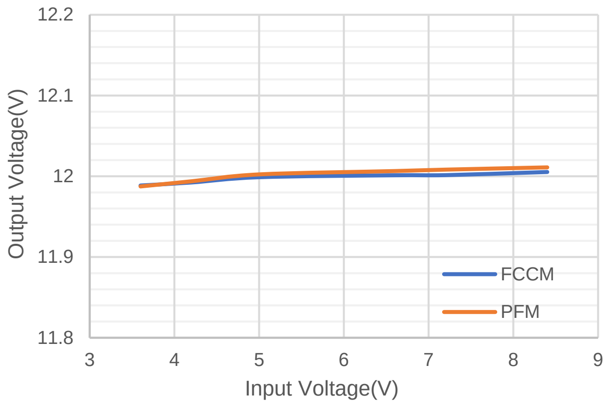


Figure 3. Line Regulation, I_{LOAD}=1A

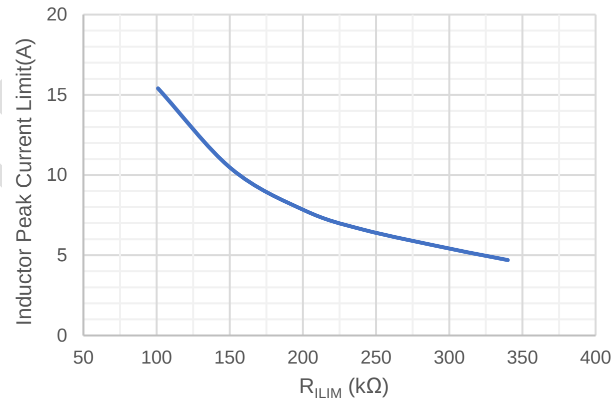


Figure 4. Peak Current Limit vs. R_{ILIM}

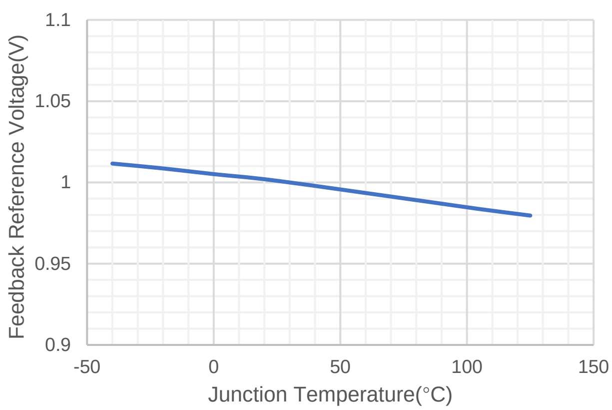


Figure 5. Reference Voltage vs. Junction Temperature

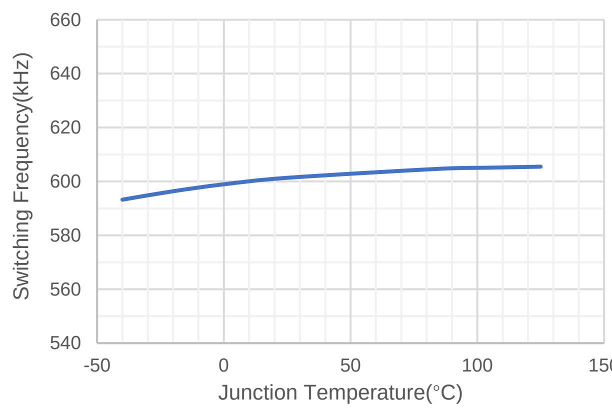


Figure 6. Switching Frequency vs. Junction Temperature

FUNCTIONAL BLOCK DIAGRAM

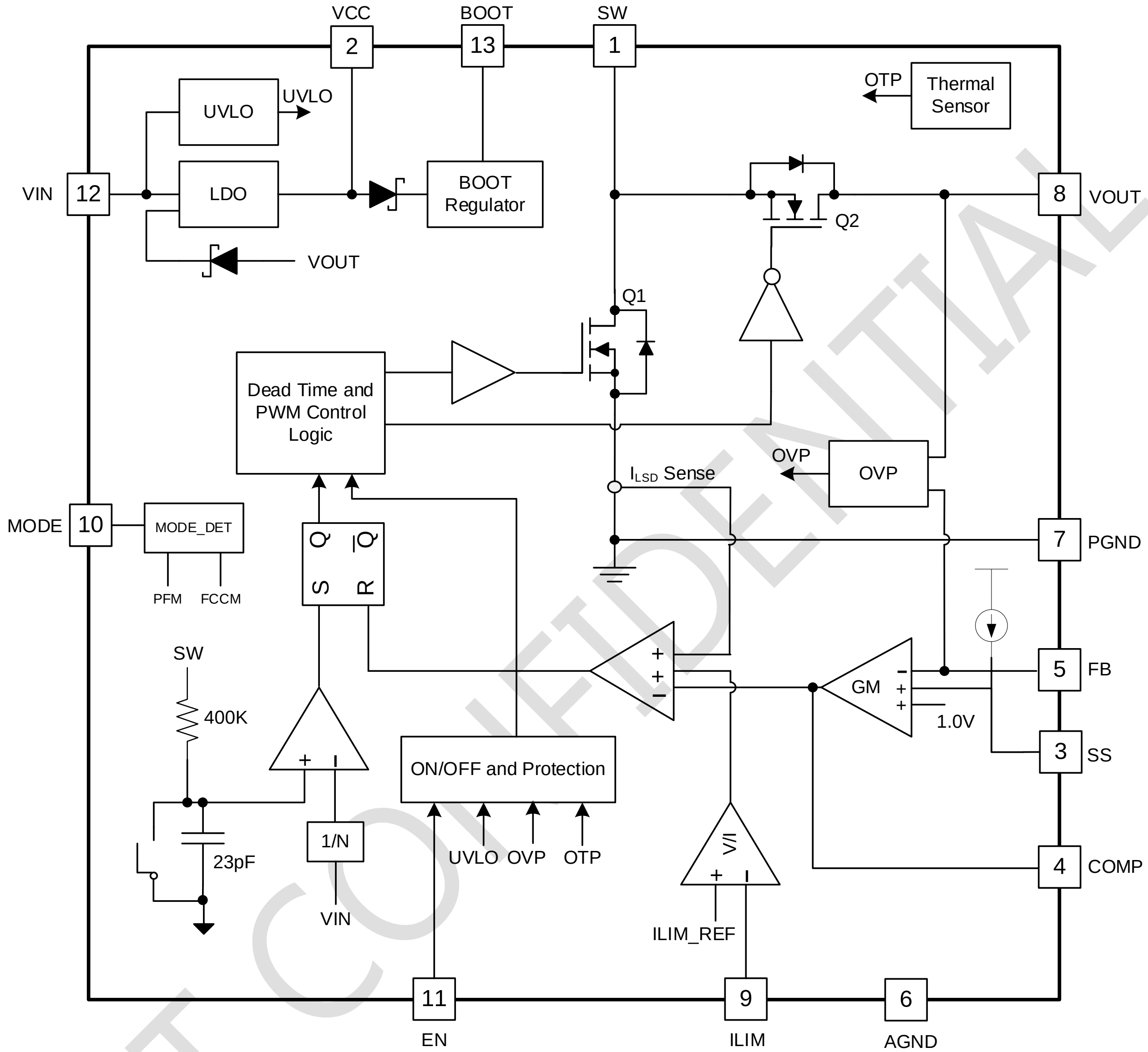


Figure 7. Functional Block Diagram

OPERATION

Overview

The SCT12A6 device is a fully integrated synchronous boost converter with programmable inductor peak current limit. The constant off-time peak current mode control provides fast transient with pseudo fixed switching frequency. When low-side MOSFET Q1 turns on, input voltage forces the inductor current rise. Sensed voltage on low-side MOSFET peak current rises above the voltage of COMP. After the inductor current reaches the peak current, the device turns off low-side MOSFET and inductor goes through body diode of high-side MOSFET Q2 during dead time. After dead time duration, the device turns on high-side MOSFET Q2 and the inductor current decreases. Based on VIN and VOUT voltage, the device predicts required off-time and turns off high-side MOSFET Q2. This repeats on cycle-by-cycle based.

The voltage feedback loop regulates the FB voltage to an internal voltage reference with an integrated trans-conductance error amplifier. The feedback loop stability and transient response are optimized through an external loop compensation network connected to the COMP pin.

The SCT12A6 can work at PFM mode to further increase the efficiency in light load condition. The quiescent current of SCT12A6 is 170uA typical with no load and no switching. Disabling the device, the typical supply shutdown current on VIN pin is 5μA.

VIN Power

The SCT12A6 is designed to operate from an input voltage supply range between 2.7 V to 20V. If the input supply is located more than a few inches from the converter, additional bulk capacitance is required in addition to the ceramic bypass capacitors. A typical choice is ceramic capacitor with a value of 47μF or 2 x 22uF.

VCC Power

The internal VCC LDO provides the bias power supply for internal circuitries. A ceramic capacitor of no less than 1uF is required to bypass from VCC pin to ground. During starting up, input of VCC LDO is from VIN pin. Once the output voltage at VOUT pin exceeds VIN voltage, VCC LDO switches its input to VOUT pin. This allows higher voltage headroom of VCC at lower input voltage. No additional components or loading are recommended on this pin.

Under Voltage Lockout UVLO

The SCT12A6 features UVLO protection for voltage rails of VIN, VCC and BOOT-SW from the converter malfunctioning and the battery over discharging. The default VIN rising threshold is 2.5V typical at startup and falling threshold is 2.3V typical at shutdown. The internal charge pump from BOOT to SW powers the gate driver to high-side MOSFET Q2. The BOOT UVLO circuit monitors the capacitor voltage between BOOT pin and SW pin. When the voltage of BOOT to SW falls below a preset threshold 3V typical, high-side MOSFET Q2 turns off. As a result, the device works as a non-synchronous boost converter.

Enable and Start-up

The SCT12A6 enables all functions and starts converter operation when EN pin is pulled high. To disable the device, EN voltage needs to fall below its low threshold. The SCT12A6 sinks a current of 5uA typical on VIN pin after shutdown. Do not float EN pin and connect it to VIN for automatic start-up.

The SCT12A6 features programmable soft start to prevent inrush current during power-up. SS pin sources an internal 8μA current charging the external soft-start capacitor C_{SS} after EN pin is pulled high. The device uses the lower voltage between the internal voltage reference 1V and the SS pin voltage as the reference input voltage of error amplifier and regulates the output. The soft-start completes when SS pin voltage exceeds the internal 1V reference. Use Equation 1 to calculate the soft-start time. When EN pin is pulled low to disable the device, the SS pin will be discharged to ground.

$$t_{SS} = \frac{C_{SS} * V_{REF}}{I_{SS}} \quad (1)$$

where

- t_{SS} is the soft start time
- V_{REF} is the internal reference voltage of 1V
- C_{SS} is the capacitance connecting to SS pin
- I_{SS} is the source current of 8uA to SS pin

Adjustable Peak Current Limit

The SCT12A6 boost converter implements cycle-by-cycle peak current limit function with sensing the internal low-side power MOSFET Q1 during overcurrent condition. While the Q1 is turned on, its conduction current is monitored by the internal sensing circuitry. Once the low-side MOSFET Q1 current exceeds the limit, it turns off immediately. An external resistor connecting ILIM pin to ground sets the low-side MOSFET Q1 peak current limit threshold. Use Equation 2 to calculate the peak current limit.

$$I_{LIM} = \frac{1500}{R_{ILIM}} \quad (2)$$

where:

- I_{LIM} is the inductor peak current limit
- R_{ILIM} is the peak current limit setting resistor in kΩ

For a typical current limit of 10A, the resistor value is 150kΩ. The minimum current limit must be higher than the required peak switch current at lowest input voltage and the highest output power not to hit the current limit and still regulate the output voltage. Notice the inductor peak current limit shall be set no higher than 16A and see Table 1 for a quick reference.

Table 1. R_{ILIM} Value for Inductor Peak Current Limit
(V_{IN}=3.6V, V_{OUT}=12V, L=1.5uH, room temperature)

I_{LIM}	R_{ILIM}
15A	100kΩ
10A	150kΩ
7.5A	200kΩ

This current limit function is realized by detecting the current flowing through the low-side MOSFET. The current limit feature loses function in the output hard short circuit conditions. At normal operation, when the output hard shorts to ground, there is a direct path to short the input voltage through high-side MOSFET Q2 or its body diode even the Q2 is turned off. This could damage the circuit components and cause catastrophic failure at load circuit.

Mode Selection

The SCT12A6 features PFM or FCCM mode at light load by MODE pin configuration. The programming information is listed in Table 2. The mode setting is latched in at each power up and is not able to be modified during operation. Cycling the input power or the EN pin can reselect the mode.

Table 2. MODE Pin Set-up for Mode Selection

MODE Pin Set-up	Connect to VCC	Connect to GND
Operation Mode	FCCM	PFM

Over Voltage Protection and Minimum On-time

The SCT12A6 features VOUT pin over voltage protection. If the VOUT pin is above 22V typical, the device stops switching immediately until the VOUT pin drops below 21 V. The OVP function prevents the connected output circuitry from un-predictive overvoltage.

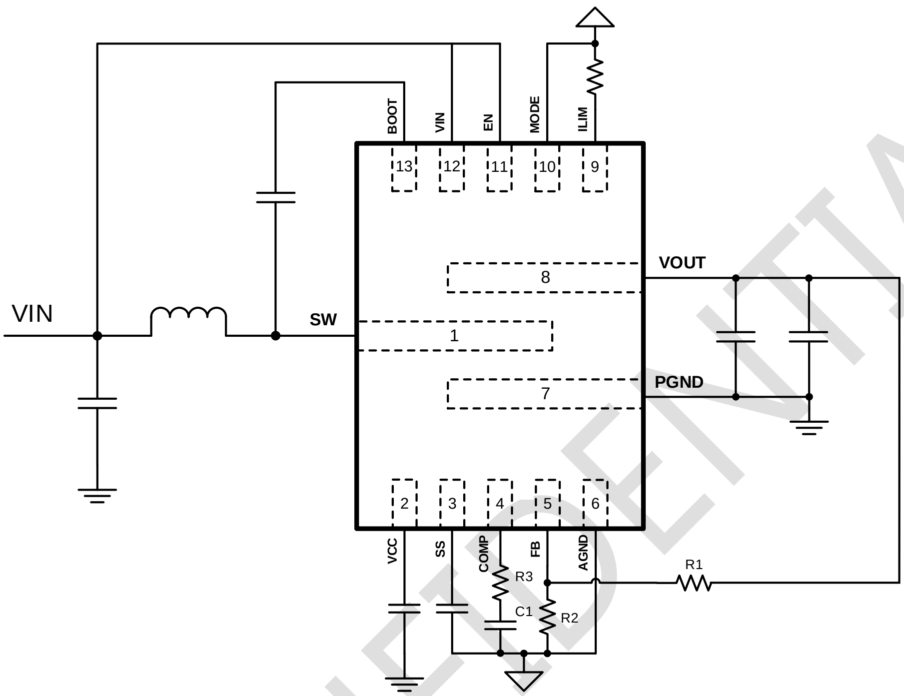
The low-side MOSFET has minimum on-time 180ns typical limitation. While the device is operating at minimum on time and further increasing Vin push output voltage beyond regulation point. With output and feedback over voltage protection, the converter skips pulse with turning off high-side MOSFET and prevents output running higher to damage the load.

Thermal Shutdown

Once the junction temperature in the SCT12A6 exceeds 175°C, the thermal sensing circuit stops switching until the junction temperature falling below 150°C, and the device restarts. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

APPLICATION INFORMATION

Typical Application



Design Parameters

Design Parameters	Example Value
Input Voltage	3.6V
Output Voltage	12V
Output Current	2A
Output voltage ripple (peak to peak)	100mV
Switching Frequency	600kHz
Operation Mode	PFM

Output Voltage

The output voltage V_{OUT} is set by an external resistor divider, R1 and R2 in typical application schematic. A minimum current of typical 20uA flowing through feedback resistor divider gives good accuracy and noise covering. The value of R1 can be calculated by Equation 3.

$$\mathrm{R1} = \frac{(V_{OUT} - V_{REF}) \times \mathrm{R2}}{V_{REF}} \quad (3)$$

where:

- V_{REF} is the feedback reference voltage for V_{OUT}, typical 1.0V

Table 3. Feedback Resistor R1 and R2 Value for Output Voltage

V_{OUT}	R1	R2
9 V	472 KΩ	59 KΩ
12 V	649 KΩ	59 KΩ
15 V	826 KΩ	59 KΩ
18 V	1 MΩ	59 KΩ

Inductor Selection

The performance of inductor affects the power supply's steady state operation, transient behavior, loop stability, and boost converter efficiency. The inductor value, DC resistance, and saturation current influences both efficiency and the magnitude of the output voltage ripple. A larger inductance value reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DC resistance, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at zero current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation.

To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, maxim load current and minimum switching frequency of the application, while considering the inductance with -30% tolerance and low power conversion efficiency.

For a boost converter, calculate the inductor DC current as in Equation 4

$$I_{LDC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (4)$$

Where

- V_{OUT} is the output voltage of the boost converter
- I_{OUT} is the output current of the boost converter
- V_{IN} is the input voltage of the boost converter
- η is the power conversion efficiency

Calculate the inductor current peak-to-peak ripple, I_{LPP}, as in Equation 5

$$I_{LPP} = \frac{1}{L \times \left(\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}}\right) \times f_{SW}} \quad (5)$$

Where

- I_{LPP} is the inductor peak-to-peak current
- L is the inductance of inductor
- f_{SW} is the switching frequency
- V_{OUT} is the output voltage

- V_{IN} is the input voltage

Therefore, the peak switching current of inductor, I_{LPEAK}, is calculated as in Equation 6.

$$I_{LPEAK} = I_{LDC} + \frac{I_{LPP}}{2} \tag{6}$$

Set the current limit of the SCT12A6 higher than the peak current I_{LPEAK} and select the inductor with the saturation current higher than the current limit.

The inductor's DC resistance (DCR), equivalent series resistance (ESR) at switching frequency and the core loss significantly affect the efficiency of power conversion. Core loss is related to the core material and different inductors have different core loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss. Usually, a data sheet of an inductor does not provide the ESR and core loss information. If needed, consult the inductor vendor for detailed information. There is a tradeoff among the inductor's inductance, DCR and ESR resistance, and its footprint. Shielded inductors typically have higher DCR than unshielded inductors. Table 4 lists recommended inductors for the SCT12A6. Verify whether the recommended inductor can support the user's target application with the previous calculations and bench evaluation.

Table 4. Recommended Inductor

Part Number	L (uH)	DCR Max (mΩ)	Saturation Current/Heat Rating Current (A)	Size Max (LxWxH mm)	Vendor
WE-HCI SMD 7443552150	1.5	5.3	17 / 14	10.5 x 10.2 x 4.0	Wurth Elektronix

Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. A 0.1μF ceramic bypass capacitor is recommended to be placed as close as possible to the VIN pin of the SCT12A6. A ceramic capacitor of more than 1μF is required at the VCC pin to get a stable operation of the internal LDO.

For the power stage, because of the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the inductor. It is recommended to have enough input capacitance to make the input voltage ripple less than 100mV. Generally, 2x 22μF input capacitance is recommended for most applications. Choose the right capacitor value carefully by considering high-capacitance ceramic capacitors DC bias effect, which has a strong influence on the final effective capacitance.

Output Capacitor Selection

For small output voltage ripple, choose a low-ESR output capacitor like a ceramic capacitor. Typically, three 22μF ceramic output capacitors work for most applications. Higher capacitor values can be used to improve the load transient response. Due to a capacitor's derating under DC bias, the bias can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. From the required output voltage ripple, use the Equation 7 and 8 to calculate the minimum required effective capacitance, C_{OUT}.

$$V_{ripple\_C} = \frac{(V_{OUT} - V_{IN\_MIN}) \times I_{OUT}}{V_{OUT} \times f_{SW} \times C_{OUT}} \tag{7}$$

$$V_{ripple\_ESR} = I_{Lpeak} \times ESR \tag{8}$$

where

- V_{ripple_C} is output voltage ripple caused by charging and discharging of the output capacitor
- V_{ripple_ESR} is output voltage ripple caused by ESR of the output capacitor
- V_{IN_MIN} is the minimum input voltage of boost converter
- V_{OUT} is the output voltage
- I_{OUT} is the output current
- I_{Lpeak} is the peak current of the inductor
- f_{SW} is the converter switching frequency
- ESR is the ESR resistance of the output capacitors

Loop Stability

An external loop compensation network comprises resister R3, ceramic capacitors C1 and C2 connected to the COMP pin to optimize the loop response of the converter. The power stage small signal loop response of constant off time with peak current control can be modeled by Equation 9.

$$G_{PS}(S) = \frac{R_{load} \times (1 - D)}{2 \times R_{SENSE}} \times \frac{(1 + \frac{S}{2\pi \times f_{ESRZ}})(1 + \frac{S}{2\pi \times f_{RHPZ}})}{1 + \frac{S}{2\pi \times f_P}} \quad (9)$$

where

- *D* is the switching duty cycle
- R_{load} is the output load resistance
- R_{SENSE} is the equivalent internal current sense resistor, which is 0.04Ω

$$f_P = \frac{1}{2\pi \times R_{load} \times C_O} \quad (10)$$

where

- C_O is the output capacitance

$$f_{PESRZ} = \frac{1}{2\pi \times ESR \times C_O} \quad (11)$$

where

- ESR is the equivalent series resistance of the output capacitor

$$f_{RHPZ} = \frac{R_{load} \times (1 - D)^2}{2\pi \times L} \quad (12)$$

The COMP pin is the output of the internal trans-conductance amplifier. Equation 13 shows the small signal transfer function of compensation network.

$$G_C(S) = \frac{G_{EA} \times R_{EA} \times V_{REF}}{V_{OUT}} \times \frac{(1 + \frac{S}{2\pi \times f_{COMZ}})}{(1 + \frac{S}{2\pi \times f_{COMP1}})(1 + \frac{S}{2\pi \times f_{COMP2}})} \quad (13)$$

where

- G_{EA} is the amplifier's trans-conductance
- R_{EA} is the amplifier's output resistance
- V_{REF} is the reference voltage at the FB pin
- V_{OUT} is the output voltage
- f_{COMP1}, f_{COMP2} are the poles' frequency of the compensation network
- f_{COMZ} is the zero's frequency of the compensation network

The next step is to choose the loop crossover frequency, f_C. The higher frequency that the loop gain stays above zero before crossing over, the faster the loop response is. It is generally accepted that the loop gain cross over no higher than the lower of either 1/10 of the switching frequency, f_{SW}, or 1/5 of the RHPZ frequency, f_{RHPZ}.

Then set the value of R3, C1, and C2 in typical application circuit by following these equations.

$$\text{R3} = \frac{2\pi \times V_{OUT} \times R_{SENSE} \times f_C \times C_O}{(1 - D) \times V_{REF} \times G_{EA}} \quad (14)$$

where

- f_C is the selected crossover frequency.

$$\text{C1} = \frac{R_{load} \times C_O}{2 \times \text{R3}} \quad (15)$$

$$\text{C2} = \frac{ESR \times C_O}{\text{R3}} \quad (16)$$

If the calculated value of C2 is less than 10pF, it can be left open. Designing the loop for greater than 45°of phase margin and greater than 10-dB gain margin eliminates output voltage ringing during the line and load transient.

Application Waveforms

V_{IN}=3.6V, V_{OUT}=12V, unless otherwise noted

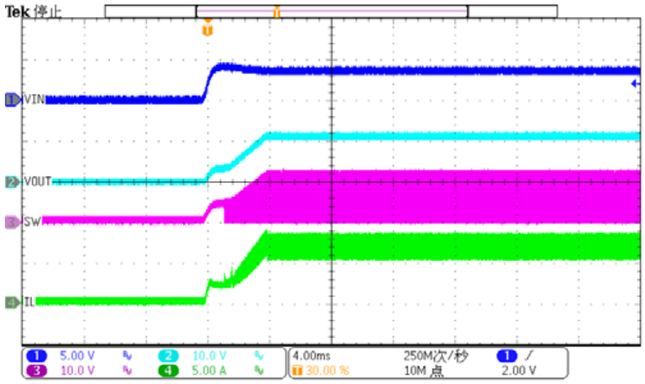


Figure 8. Power up (I_{LOAD}=2A)

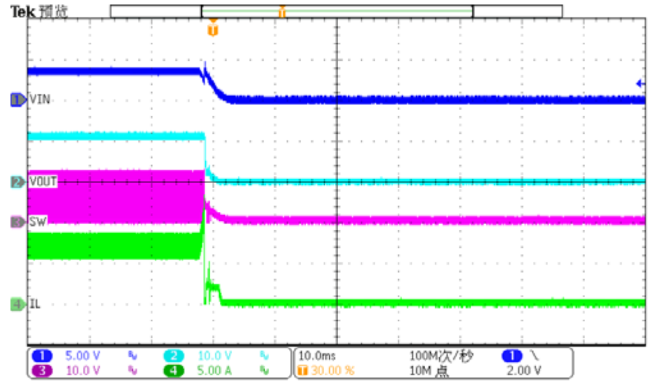


Figure 9. Power down (I_{LOAD}=2A)

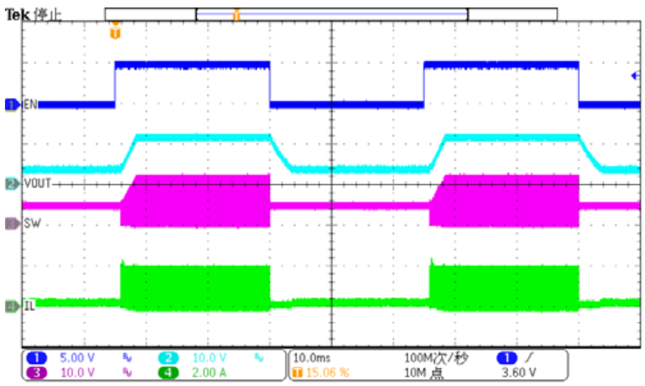


Figure 10. EN toggle (I_{LOAD}=0.1A)

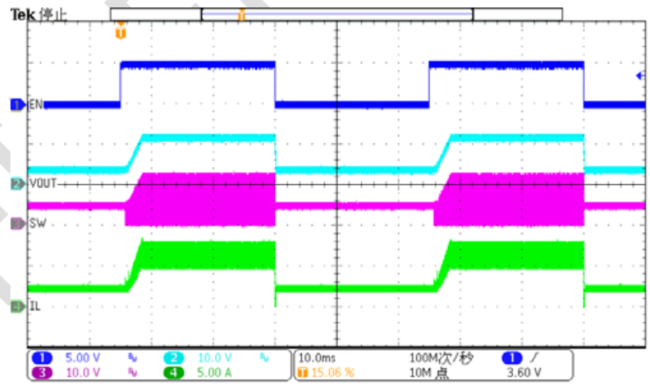


Figure 11. EN toggle (I_{LOAD}=2A)

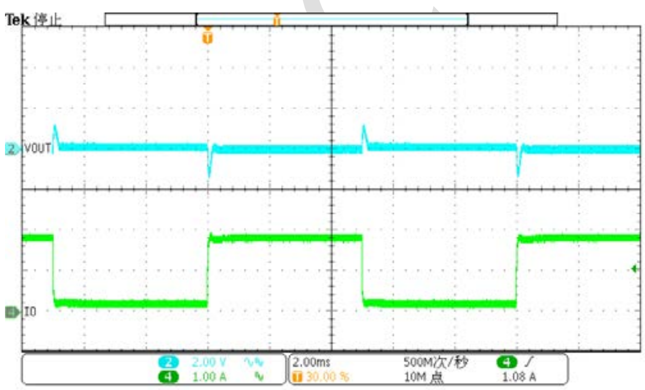


Figure 12. Load Transient (0.2A-1.8A)

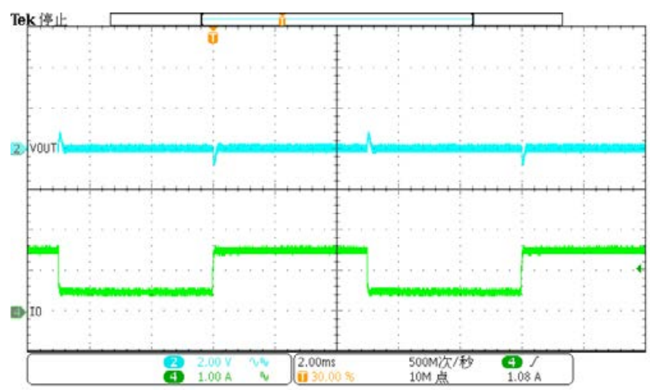


Figure 13. Load Transient (0.25A-1.5A)

Application Waveforms

V_{IN}=3.6V, V_{OUT}=12V, unless otherwise noted

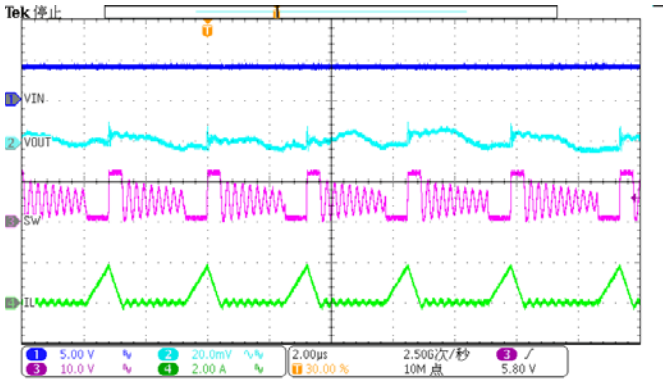


Figure 14. Output Ripple (I_{LOAD}=100mA, PFM)

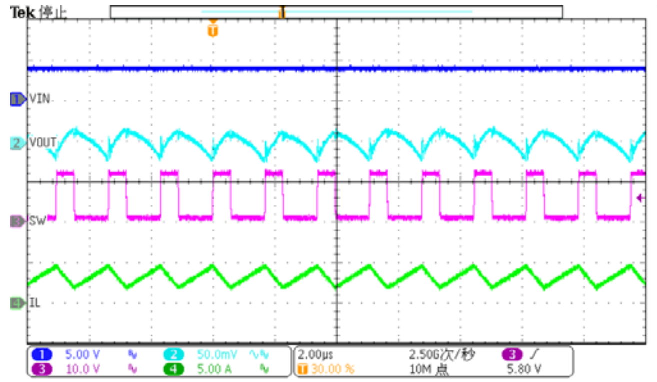


Figure 15. Output Ripple (I_{LOAD}=1A)

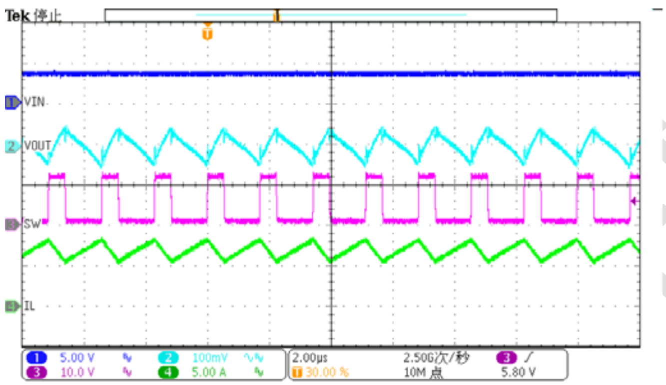


Figure 16. Output Ripple (I_{LOAD}=2A)

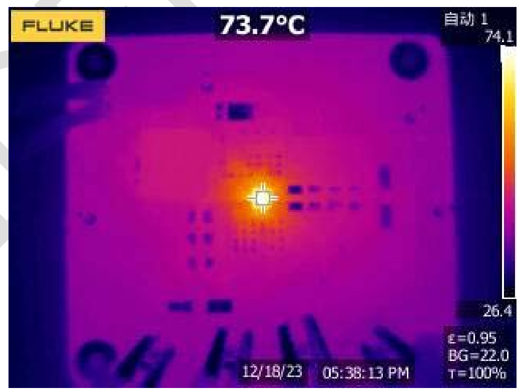


Figure 17. Thermal, 3.6V_{IN}, 12V_{OUT}, 2A

Layout Guideline

The regulator could suffer from instability and noise problems without careful layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be close to the VIN pin and ground pad to reduce the input supply ripple. The placement and ground trace for the output capacitor is critical for the performance of SW ringing voltage. Place the output capacitor as close to VOUT pins and power ground pad as possible to reduce high frequency ringing voltage on SW pin.

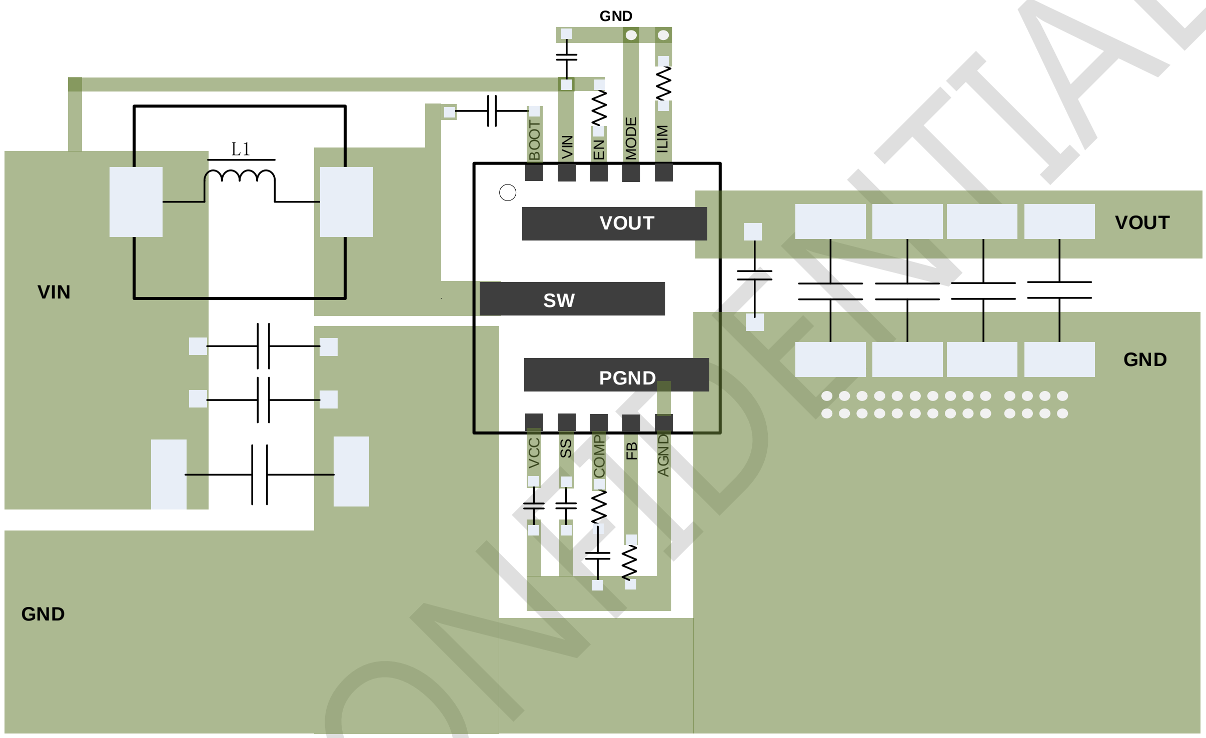


Figure 18. PCB Layout Example Top Layer

Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation 17.

$$P_{D(MAX)} = \frac{125 - T_A}{R_{\theta JA}} \quad (17)$$

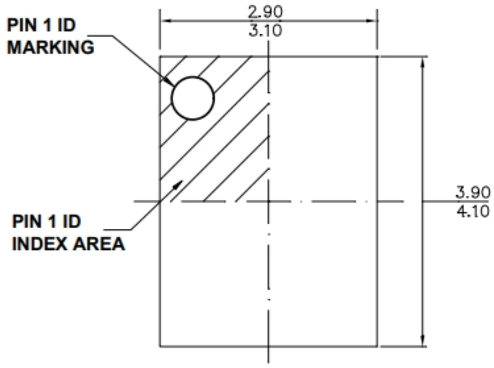
where

- T_A is the maximum ambient temperature for the application
- $R_{\theta JA}$ is the junction-to-ambient thermal resistance given in the Thermal Information table

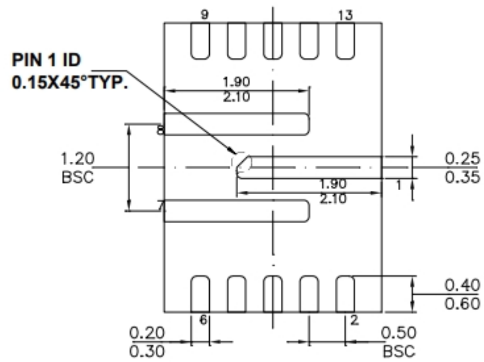
The real junction-to-ambient thermal resistance $R_{\theta JA}$ of the package greatly depends on the PCB type, layout, thermal pad connection and environmental factor. Using thick PCB copper and soldering the thermal pad to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.

PACKAGE INFORMATION

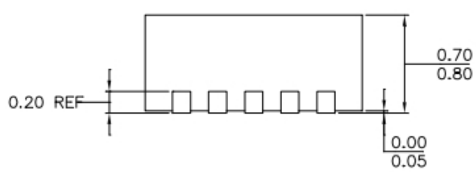
PACKAGE OUTLINE DRAWING FOR 13L FCTQFN (3.0X4.0MM)
POD-0046 Revision 0.0



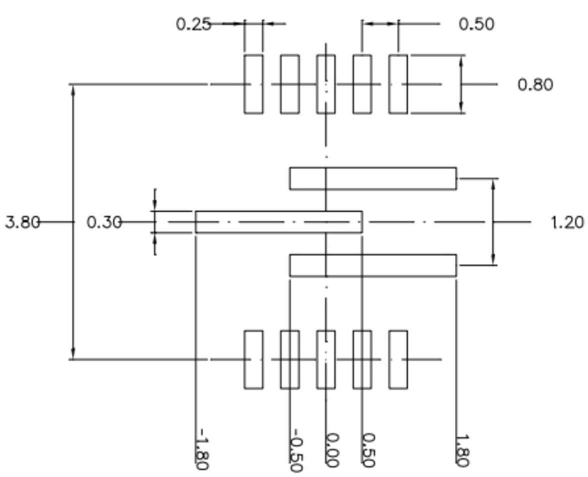
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

TAPE AND REEL INFORMATION